

# 采用小型封装且具有 $\pm 15\text{kV}$ IEC ESD 保护的 TRS3232E 3V 至 5.5V 多通道 RS-232 线路驱动器和接收器

## 1 特性

- 为 RS-232 总线引脚提供 ESD 保护
  - $\pm 15\text{kV}$  HBM
  - $\pm 8\text{kV}$  ( IEC61000-4-2, 接触放电 )
  - $\pm 15\text{kV}$  ( IEC61000-4-2, 气隙放电 )
- 符合或超出 TIA/EIA-232-F 和 ITU V.28 标准的要求
- 由 3V 至 5.5V  $V_{CC}$  电源供电
  - 可与低至 2.7V  $V_{CC}$  的 RS-232 交互操作
- 运行速率高达 250kbps
- 两个驱动器和两个接收器
- 低电源电流: 300  $\mu\text{A}$  ( 典型值 )
- 外部电容器:  $4 \times 0.1 \mu\text{F}$
- 接受 5V 逻辑输入及 3.3V 电源
- 采用近似于芯片级封装 (QFN-16, 3mm  $\times$  3mm), 比 SOIC-16 小 85%
- 与备选高速器件兼容的引脚 (1Mbps)
  - SN65C3232E (  $-40^{\circ}\text{C}$  至  $+85^{\circ}\text{C}$  )
  - SN75C3232E (  $0^{\circ}\text{C}$  至  $70^{\circ}\text{C}$  )

## 2 应用

- 工业 PC
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- 笔记本电脑
- 掌上电脑
- 手持设备

## 3 说明

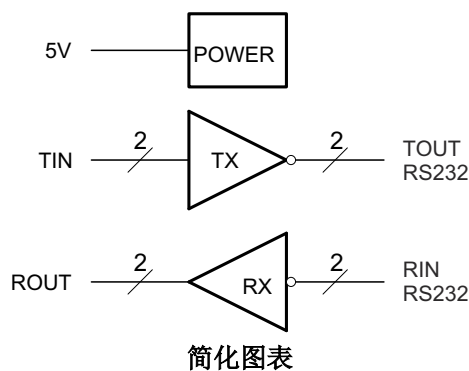
TRS3232E 器件由两个线路驱动器、两个线路接收器和一个双路电荷泵电路组成, 具有引脚对引脚 ( 串行端口连接引脚, 包括 GND )  $\pm 15\text{kV}$  IEC ESD 保护。

该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。这些器件以高达 250kbps 的数据信号传输速率和最大值为  $30\text{V}/\mu\text{s}$  的驱动器输出压摆率运行。

### 器件信息<sup>(1)</sup>

| 器件型号     | 封装              | 封装尺寸 ( 标称值 )            |
|----------|-----------------|-------------------------|
| TRS3232E | SOIC (D) 16     | 9.90mm $\times$ 3.91mm  |
|          | SSOP (DB) (16)  | 6.20mm $\times$ 5.30mm  |
|          | SOIC (DW) (16)  | 10.30mm $\times$ 7.50mm |
|          | TSSOP (PW) 16   | 5.00mm $\times$ 4.40mm  |
|          | VQFN (RGT) (16) | 3.00mm $\times$ 3.00mm  |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| <b>Changes from Revision C (June 2021) to Revision D (June 2021)</b>                                                         | <b>Page</b> |
|------------------------------------------------------------------------------------------------------------------------------|-------------|
| • 添加了应用工业 PC、有线网络、数据中心和企业级计算.....                                                                                            | 1           |
| • Changed the table note in the <i>ESD Ratings - IEC Specifications</i> to make it applicable to D, DB and PW packages. .... | 4           |
| • Changed the thermal parameter values for D, DB and PW packages in the <i>Thermal Information</i> table.....                | 5           |
| <b>Changes from Revision B (October 2017) to Revision C (June 2021)</b>                                                      | <b>Page</b> |
| • 向器件信息 添加了 RGT 封装 .....                                                                                                     | 1           |
| • Added the RGT <i>Pin Configuration</i> .....                                                                               | 3           |
| • Added the <i>ESD Ratings - IEC Specifications</i> .....                                                                    | 4           |
| • Added RGT to the <i>Thermal Information</i> .....                                                                          | 5           |
| • Added RGT package to the <i>Switching Characteristics</i> .....                                                            | 7           |
| • Changed the capacitor value From: 1 µf To: 0.1 µf in the <i>Layout Diagram</i> .....                                       | 15          |
| <b>Changes from Revision A (July 2015) to Revision B (October 2017)</b>                                                      | <b>Page</b> |
| • 添加了特性：可与低至 2.7V V <sub>CC</sub> 的 RS-232 交互操作.....                                                                         | 1           |
| • Added 图 6-3 .....                                                                                                          | 0           |
| <b>Changes from Revision * (April 2007) to Revision A (July 2015)</b>                                                        | <b>Page</b> |
| • 删除了 订购信息 表.....                                                                                                            | 1           |
| • 添加了器件信息表、引脚配置和功能部分、ESD 等级表、热性能信息表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.                            | 1           |

## 5 Pin Configuration and Functions

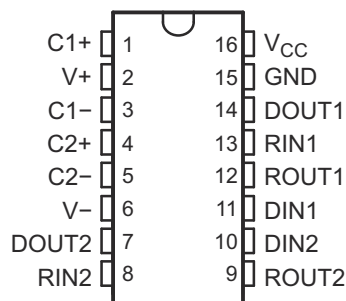


图 5-1. D, DW, DB or PW Package, 16-Pin SOIC, SSOP or TSSOP, Top View

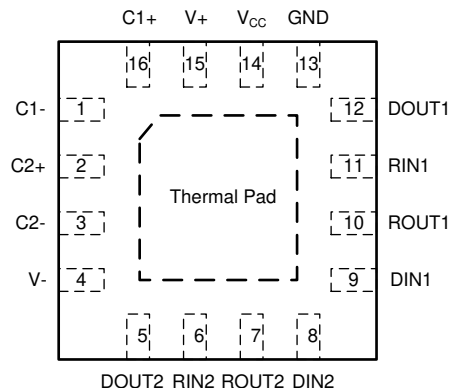


图 5-2. RGT package, 16 Pin VQFN, Top View

表 5-1. Pin Functions

| PIN             |     | RGT | I/O | DESCRIPTION                                                                           |
|-----------------|-----|-----|-----|---------------------------------------------------------------------------------------|
| NAME            | NO. |     |     |                                                                                       |
| C1+             | 1   | 16  | —   | Positive lead of C1 capacitor                                                         |
| C1 -            | 3   | 1   | —   | Negative lead of C1 capacitor                                                         |
| C2+             | 4   | 2   | —   | Positive lead of C2 capacitor                                                         |
| C2 -            | 5   | 3   | —   | Negative lead of C2 capacitor                                                         |
| DIN1            | 11  | 9   | I   | Logic data input (from UART)                                                          |
| DIN2            | 10  | 8   | I   | Logic data input (from UART)                                                          |
| DOUT2           | 7   | 5   | O   | RS232 line data output (to remote RS232 system)                                       |
| DOUT1           | 14  | 12  | O   | RS232 line data output (to remote RS232 system)                                       |
| GND             | 15  | 13  | —   | Ground                                                                                |
| RIN1            | 13  | 11  | I   | RS232 line data input (from remote RS232 system)                                      |
| RIN2            | 8   | 6   | I   | RS232 line data input (from remote RS232 system)                                      |
| ROUT2           | 9   | 7   | O   | Logic data output (to UART)                                                           |
| ROUT1           | 12  | 10  | O   | Logic data output (to UART)                                                           |
| V+              | 2   | 15  | O   | Positive charge pump output for storage capacitor only                                |
| V -             | 6   | 4   | O   | Negative charge pump output for storage capacitor only                                |
| V <sub>CC</sub> | 16  | 14  | —   | Supply voltage, connect to external 3-V to 5.5-V power supply                         |
| Thermal Pad     |     | Yes | —   | Thermal pad for improving heat dissipation. Can be connected to GND or left floating. |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                               |           | MIN    | MAX                   | UNIT |
|------------------|-----------------------------------------------|-----------|--------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage <sup>(2)</sup>                 |           | – 0.3  | 6                     | V    |
| V+               | Positive output supply voltage <sup>(2)</sup> |           | – 0.3  | 7                     | V    |
| V –              | Negative output supply voltage <sup>(2)</sup> |           | 0.3    | – 7                   | V    |
| V+ – V –         | Supply voltage difference <sup>(2)</sup>      |           |        | 13                    | V    |
| V <sub>I</sub>   | Input voltage                                 | Drivers   | – 0.3  | 6                     | V    |
|                  |                                               | Receivers | – 25   | 25                    | V    |
| V <sub>O</sub>   | Output voltage                                | Drivers   | – 13.2 | 13.2                  | V    |
|                  |                                               | Receivers | – 0.3  | V <sub>CC</sub> + 0.3 | V    |
| T <sub>J</sub>   | Operating virtual junction temperature        |           |        | 150                   | °C   |
| T <sub>stg</sub> | Storage temperature                           |           | – 65   | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 6.2 ESD Ratings

|                    |                         |                                                                                |                                             | VALUE  | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|---------------------------------------------|--------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | All pins except RIN1, RIN2, DOUT1 and DOUT2 | ±2000  | V    |
|                    |                         |                                                                                | Pins RIN1, RIN2, DOUT1 and DOUT2            | ±15000 |      |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | All pins                                    | ±1500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings - IEC Specifications

|                    |                         |                                                 |                               | VALUE  | UNIT |
|--------------------|-------------------------|-------------------------------------------------|-------------------------------|--------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | IEC 61000-4-2, Contact Discharge <sup>(1)</sup> | Pins RIN1, RIN2, DOUT1, DOUT2 | ±8000  | V    |
|                    |                         | IEC 61000-4-2, Air-Gap Discharge <sup>(1)</sup> | Pins RIN1, RIN2, DOUT1, DOUT2 | ±15000 |      |

- (1) For RGT, D, DB and PW packages only: Minimum of 1-μF capacitor between VCC and GND is required to meet the specified IEC 61000-4-2 rating.

## 6.4 Recommended Operating Conditions

See 图 9-1.<sup>(1)</sup>

|                                          |     |                         | MIN  | NOM | MAX | UNIT |
|------------------------------------------|-----|-------------------------|------|-----|-----|------|
| Supply voltage                           |     | $V_{CC} = 3.3\text{ V}$ | 3    | 3.3 | 3.6 | V    |
|                                          |     | $V_{CC} = 5\text{ V}$   | 4.5  | 5   | 5.5 |      |
| $V_{IH}$ Driver high-level input voltage | DIN | $V_{CC} = 3.3\text{ V}$ | 2    |     | 5.5 | V    |
|                                          |     | $V_{CC} = 5\text{ V}$   | 2.4  |     | 5.5 |      |
| $V_{IL}$ Driver low-level input voltage  | DIN |                         | 0    |     | 0.8 | V    |
| $V_I$ Receiver input voltage             | RIN |                         | - 25 |     | 25  | V    |
| $T_A$ Operating free-air temperature     |     | TRS3232EC               | 0    |     | 70  | °C   |
|                                          |     | TRS3232EI               | - 40 |     | 85  |      |

(1)  $C_1 - C_4 = 0.1\text{ }\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ;  $C_1 = 0.047\text{ }\mu\text{F}$ ,  $C_2 - C_4 = 0.33\text{ }\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

## 6.5 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TRS3232E      |          |           |           |               | UNIT |
|-------------------------------|----------------------------------------------|---------------|----------|-----------|-----------|---------------|------|
|                               |                                              | PW<br>(TSSOP) | D (SOIC) | DW (SOIC) | DB (SSOP) | RGT<br>(VQFN) |      |
|                               |                                              | 16 PINS       | 16 PINS  | 16 PINS   | 16 PINS   | 16 PINS       |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 108.2         | 85.9     | 72.3      | 103.1     | 48.8          | °C/W |
| $R_{\theta JCTop}$            | Junction-to-case (top) thermal resistance    | 39.0          | 43.1     | 33.5      | 49.2      | 55.8          | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 54.4          | 44.5     | 37.1      | 54.8      | 23.2          | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 3.3           | 10.1     | 7.5       | 12.0      | 1.7           | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 53.8          | 44.1     | 37.1      | 54.1      | 23.2          | °C/W |
| $R_{\theta JCbot}$            | Junction-to-case (bottom) thermal resistance | N/A           | N/A      | N/A       | N/A       | 9.0           | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.6 Electrical Characteristics — Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 9-1).<sup>(1)</sup>

| PARAMETER                      | TEST CONDITIONS                         | MIN | TYP <sup>(2)</sup> | MAX | UNIT |
|--------------------------------|-----------------------------------------|-----|--------------------|-----|------|
| I <sub>CC</sub> Supply current | No load, V <sub>CC</sub> = 3.3 V or 5 V |     | 0.3                | 1   | mA   |

- (1) Test conditions are C1 – C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2 – C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.  
 (2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.7 Electrical Characteristics — Driver

over operating free-air temperature range (unless otherwise noted) (see 图 9-1).<sup>(1)</sup>

| PARAMETER                                                   | TEST CONDITIONS                                                                         | MIN | TYP <sup>(2)</sup> | MAX      | UNIT     |
|-------------------------------------------------------------|-----------------------------------------------------------------------------------------|-----|--------------------|----------|----------|
| V <sub>OH</sub> High-level output voltage                   | DOUT at R <sub>L</sub> = 3 k $\Omega$ to GND, DIN = GND                                 | 5   | 5.4                |          | V        |
| V <sub>OL</sub> Low-level output voltage                    | DOUT at R <sub>L</sub> = 3 k $\Omega$ to GND, DIN = V <sub>CC</sub>                     | – 5 | – 5.4              |          | V        |
| I <sub>IH</sub> High-level input current                    | V <sub>I</sub> = V <sub>CC</sub>                                                        |     | $\pm$ 0.01         | $\pm$ 1  | $\mu$ A  |
| I <sub>IL</sub> Low-level input current                     | V <sub>I</sub> at GND                                                                   |     | $\pm$ 0.01         | $\pm$ 1  | $\mu$ A  |
| I <sub>OS</sub> <sup>(3)</sup> Short-circuit output current | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V                                           |     | $\pm$ 35           | $\pm$ 60 | mA       |
|                                                             | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V                                           |     |                    |          |          |
| r <sub>O</sub> Output resistance                            | V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = $\pm$ 2 V | 300 | 10M                |          | $\Omega$ |

- (1) Test conditions are C1 – C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2 – C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.  
 (2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.  
 (3) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.8 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 9-1).<sup>(2)</sup>

| PARAMETER                                                                | TEST CONDITIONS                | MIN                   | TYP <sup>(1)</sup>    | MAX | UNIT |
|--------------------------------------------------------------------------|--------------------------------|-----------------------|-----------------------|-----|------|
| V <sub>OH</sub> High-level output voltage                                | I <sub>OH</sub> = -1 mA        | V <sub>CC</sub> - 0.6 | V <sub>CC</sub> - 0.1 |     | V    |
| V <sub>OL</sub> Low-level output voltage                                 | I <sub>OL</sub> = 1.6 mA       |                       |                       | 0.4 | V    |
| V <sub>IT+</sub> Positive-going input threshold voltage                  | V <sub>CC</sub> = 3.3 V        |                       | 1.5                   | 2.4 | V    |
|                                                                          | V <sub>CC</sub> = 5 V          |                       | 1.8                   | 2.4 |      |
| V <sub>IT-</sub> Negative-going input threshold voltage                  | V <sub>CC</sub> = 3.3 V        | 0.6                   | 1.2                   |     | V    |
|                                                                          | V <sub>CC</sub> = 5 V          | 0.8                   | 1.5                   |     |      |
| V <sub>hys</sub> Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> ) |                                |                       | 0.3                   |     | V    |
| r <sub>i</sub> Input resistance                                          | V <sub>I</sub> = ±3 V to ±25 V | 3                     | 5                     | 7   | kΩ   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Test conditions are C1 - C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.9 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 9-1).<sup>(1)</sup>

| PARAMETER                                                                   | TEST CONDITIONS                                                                   | MIN                                | TYP <sup>(2)</sup> | MAX | UNIT |
|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------------|------------------------------------|--------------------|-----|------|
| Maximum data rate                                                           | R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 1000 pF, see 图 7-1<br>One DOUT switching, | RGT package<br>250                 | 500                |     | kbps |
|                                                                             |                                                                                   | D, DB, DW and PW packages<br>150   | 250                |     |      |
| t <sub>sk(p)</sub> Driver pulse skew <sup>(3)</sup>                         | R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 1000 pF, V <sub>CC</sub> = 5 V 图 7-2      | RGT package                        | 50                 |     | ns   |
|                                                                             | R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 150 pF to 2500 pF see 图 7-2       | D, DB, DW and PW packages          | 300                |     |      |
| SR(tr) Driver slew rate, transition region (see 图 7-1)                      | R <sub>L</sub> = 3 kΩ to 7 kΩ, V <sub>CC</sub> = 3.3 V                            | C <sub>L</sub> = 150 pF to 1000 pF | 6                  | 30  | V/μs |
|                                                                             |                                                                                   | C <sub>L</sub> = 150 pF to 2500 pF | 4                  | 30  |      |
| t <sub>PLH</sub> Receiver propagation delay time, low- to high-level output | C <sub>L</sub> = 150 pF, see 图 7-3                                                | RGT package                        | 90                 |     | ns   |
|                                                                             |                                                                                   | D, DB, DW and PW packages          | 300                |     |      |
| t <sub>PHL</sub> Receiver propagation delay time, high- to low-level output | C <sub>L</sub> = 150 pF, see 图 7-3                                                | RGT package                        | 100                |     | ns   |
|                                                                             |                                                                                   | D, DB, DW and PW packages          | 300                |     |      |
| t <sub>sk(p)</sub> Receiver pulse skew <sup>(3)</sup>                       | RGT package                                                                       |                                    | 20                 |     | ns   |
|                                                                             | D, DB, DW and PW packages                                                         |                                    | 300                |     |      |

(1) Test conditions are C1 - C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

## Typical Characteristics

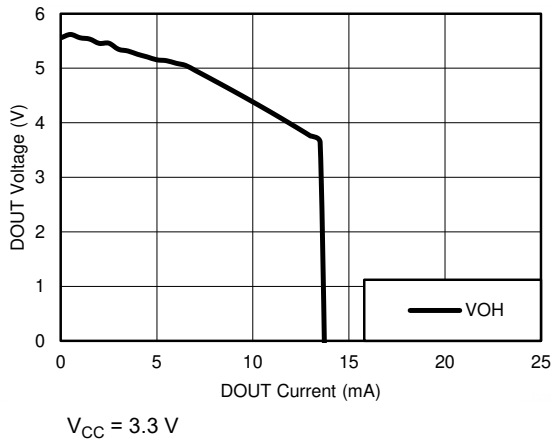


图 6-1. DOUT  $V_{OH}$  vs Load Current, Both Drivers Loaded

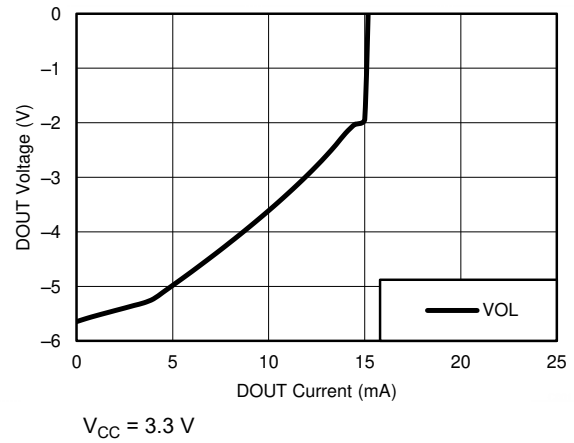


图 6-2. DOUT  $V_{OL}$  vs Load Current, Both Drivers Loaded

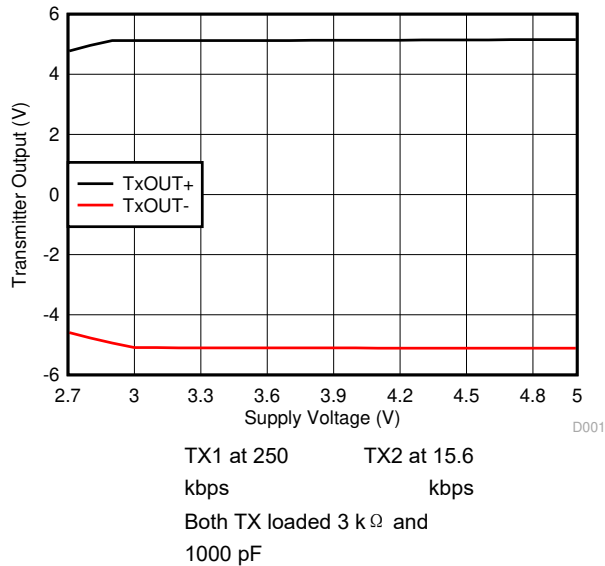


图 6-3. Driver Output Voltage vs. Supply Voltage, Both Drivers Loaded

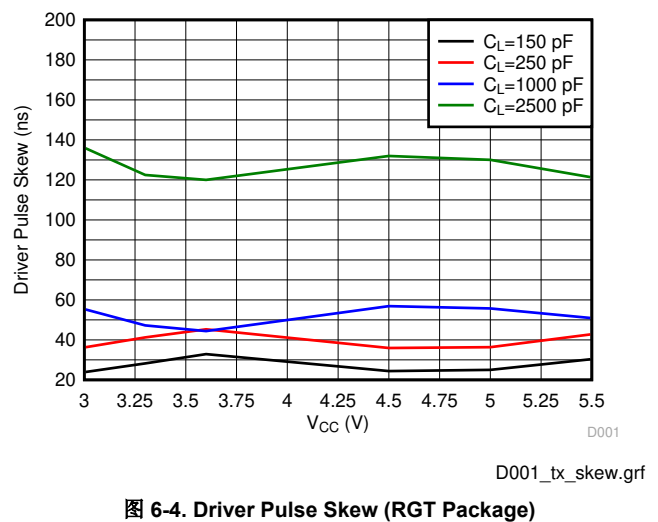


图 6-4. Driver Pulse Skew (RGT Package)

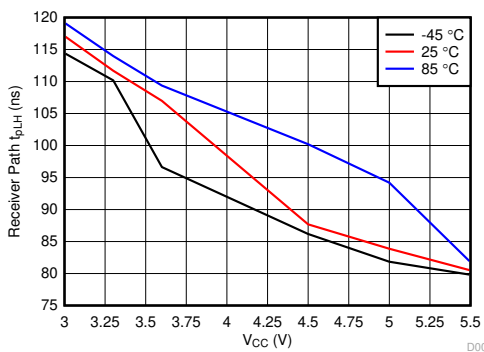


图 6-5. Receiver Path Low-to-High Propagation Delay (RGT Package)

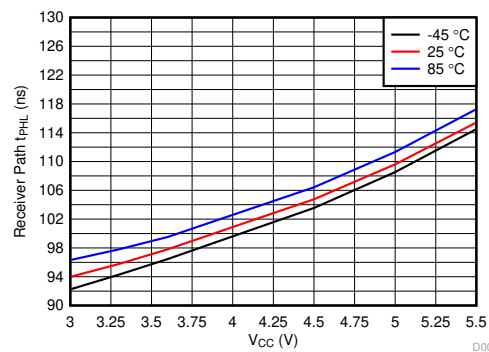
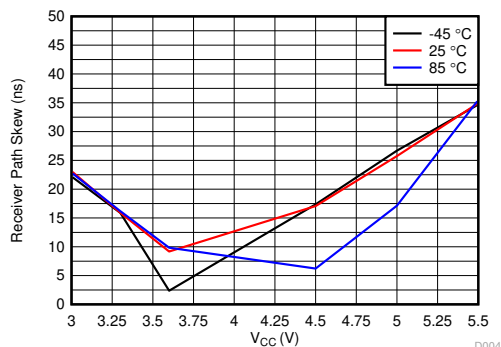


图 6-6. Receiver Path High-to-Low Propagation Delay (RGT Package)

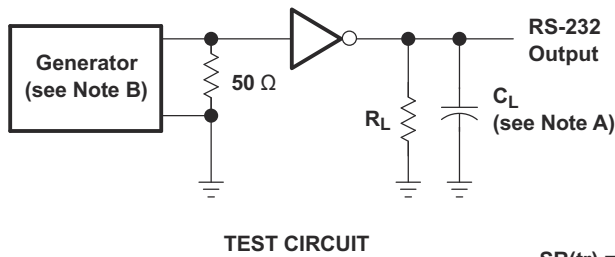
## Typical Characteristics



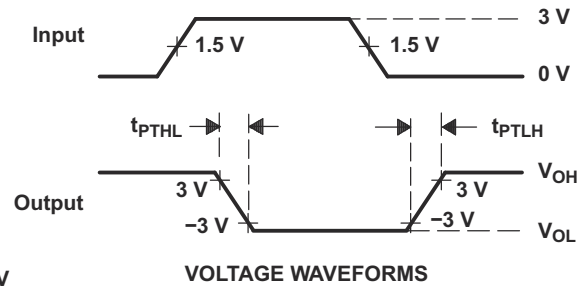
D004\_rx\_skew.grf

图 6-7. Receiver Path Skew ( $|t_{pHL} - t_{pLH}|$ ) (RGT Package)

## 7 Parameter Measurement Information



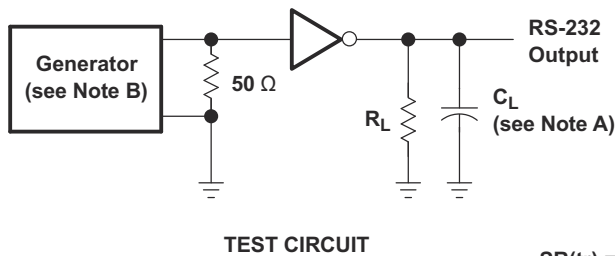
$$SR(tr) = \frac{6\text{ V}}{t_{PTHL} \text{ or } t_{PTLH}}$$



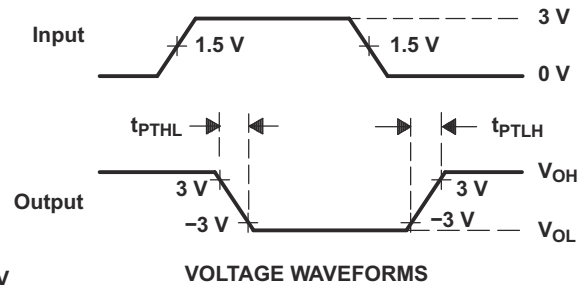
A.  $C_L$  includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbps,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

图 7-1. Driver Slew Rate



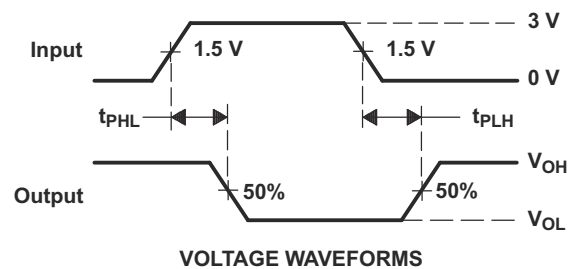
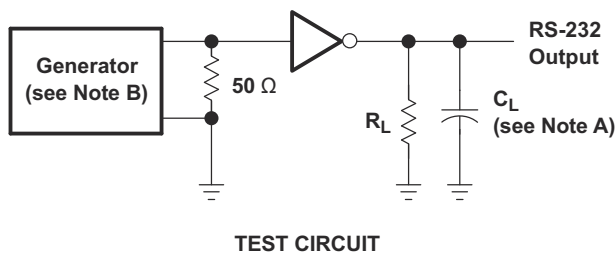
$$SR(tr) = \frac{6\text{ V}}{t_{PTHL} \text{ or } t_{PTLH}}$$



A.  $C_L$  includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbps,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

图 7-2. Driver Pulse Skew



A.  $C_L$  includes probe and jig capacitance

B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

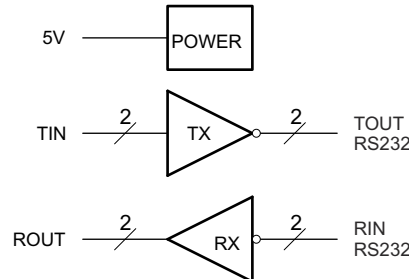
图 7-3. Receiver Propagation Delay Times

## 8 Detailed Description

### 8.1 Overview

The TRS3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbps and a maximum of 30-V/ $\mu$ s driver output slew rate. Outputs are protected against shorts to ground.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors.

#### 8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

#### 8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

## 8.4 Device Functional Modes

表 8-1 和 表 8-2 list the functional modes of the drivers and receivers of TRS3232E.

表 8-1. Each Driver<sup>(1)</sup>

| INPUT<br>DIN | OUTPUT<br>DOUT |
|--------------|----------------|
| L            | H              |
| H            | L              |

(1) H = high level, L = low level

表 8-2. Each Receiver<sup>(1)</sup>

| INPUT<br>RIN | OUTPUT<br>ROUT |
|--------------|----------------|
| L            | H              |
| H            | L              |
| Open         | H              |

(1) H = high level, L = low level,  
Open = input disconnected or connected driver off

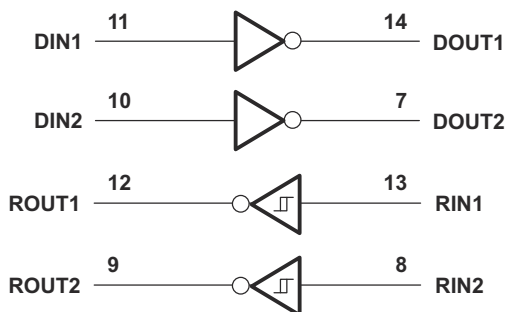


图 8-1. Logic Diagram

### 8.4.1 V<sub>CC</sub> Powered by 3 V to 5.5 V

The device is in normal operation.

### 8.4.2 V<sub>CC</sub> Unpowered, V<sub>CC</sub> = 0 V

When TRS3232E is unpowered, it can be safely connected to an active remote RS232 device.

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

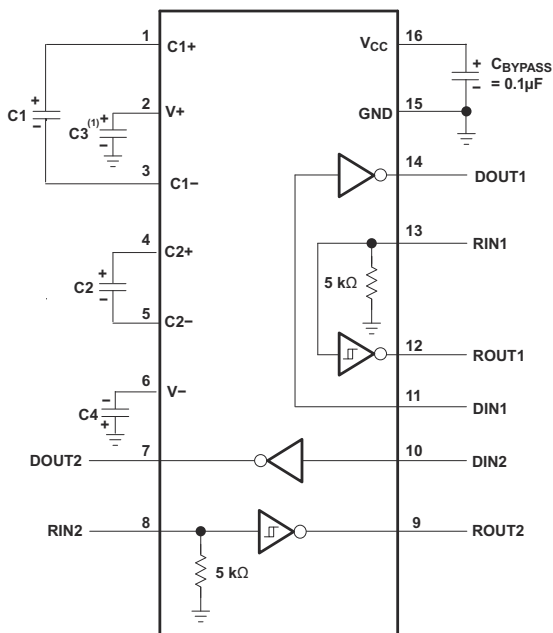
### 9.1 Application Information

The TRS3232E interfaces logic lines from a UART or microcontroller to the voltage and current levels needed for RS232 communication. The TIN inputs will accept 5-V logic with 3.3-V  $V_{CC}$  supply. All baud rates up to 250-kbps are supported.

It is important to use the correct capacitors for the  $V_{CC}$  voltage. This will reduce ripple voltage on the TOUT outputs. If only one driver is needed, the unused driver input should be connected to  $V_{CC}$  or ground.

### 9.2 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable. For proper operation, add capacitors as shown in 表 9-1.



A. C3 can be connected to  $V_{CC}$  or GND

Resistor values shown are nominal.

Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**图 9-1. Typical Operating Circuit and Capacitor Values**

**表 9-1.  $V_{CC}$  vs Capacitor Values**

| $V_{CC}$          | C1            | C2, C3, C4   |
|-------------------|---------------|--------------|
| 3.3 V $\pm$ 0.3 V | 0.1 $\mu$ F   | 0.1 $\mu$ F  |
| 5 V $\pm$ 0.5 V   | 0.047 $\mu$ F | 0.33 $\mu$ F |
| 3 V $\pm$ 5.5 V   | 0.1 $\mu$ F   | 0.47 $\mu$ F |

### 9.2.1 Design Requirements

The recommended  $V_{CC}$  is 3.3 V or 5 V. 3 V to 5.5 V is also possible.

The maximum recommended bit rate is 250 kbps.

### 9.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on  $V_{CC}$  level for best performance.

### 9.2.3 Application Curve

图 9-2 curves are for 3.3-V  $V_{CC}$  and 250-kbps alternative bit data stream.

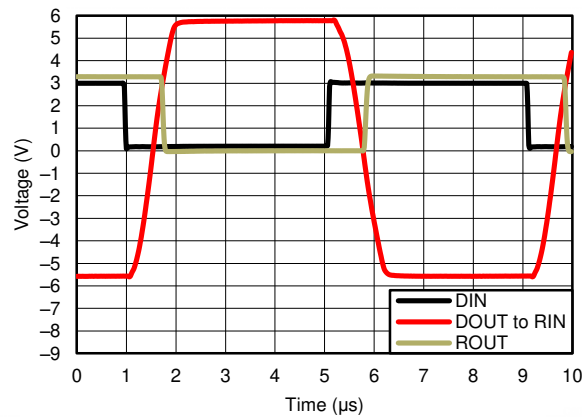


图 9-2. 250 kbps Driver to Receiver Loopback Timing Waveform,  $V_{CC} = 3.3$  V

## 10 Power Supply Recommendations

The supply voltage,  $V_{CC}$ , should be between 3 V and 5.5 V. Select the values of the charge-pump capacitors using 表 9-1.

## 11 Layout

### 11.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

### 11.2 Layout Example

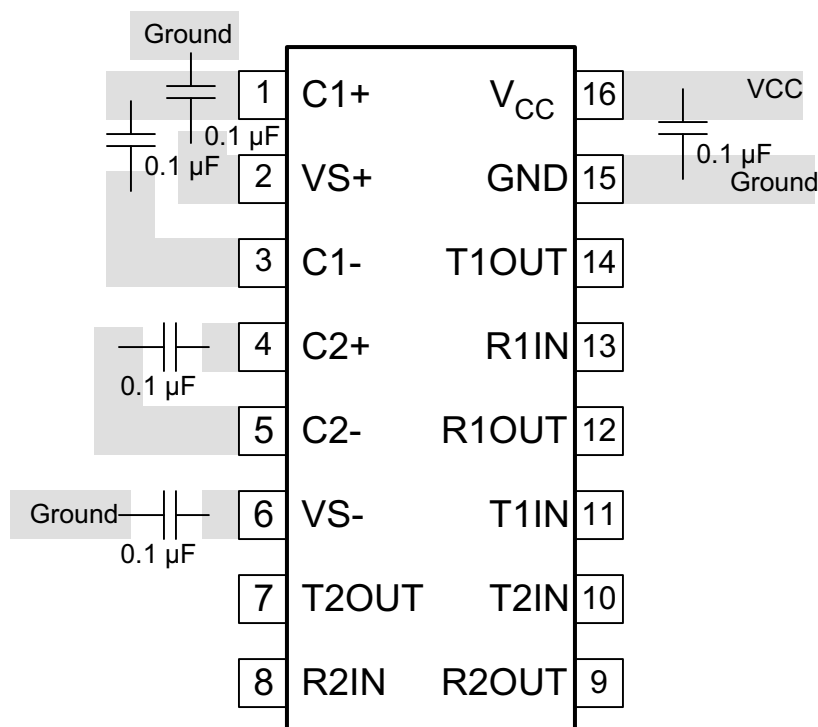


图 11-1. Layout Diagram

## 12 Device and Documentation Support

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 12.3 Trademarks

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### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TRS3232ECDR      | ACTIVE        | SOIC         | D                  | 16   | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | TRS3232EC               | <a href="#">Samples</a> |
| TRS3232ECDW      | NRND          | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | TRS3232EC               |                         |
| TRS3232ECDWR     | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | TRS3232EC               | <a href="#">Samples</a> |
| TRS3232ECPWR     | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | RS32EC                  | <a href="#">Samples</a> |
| TRS3232EIDBR     | ACTIVE        | SSOP         | DB                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | RS32EI                  | <a href="#">Samples</a> |
| TRS3232EIDR      | ACTIVE        | SOIC         | D                  | 16   | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | TRS3232EI               | <a href="#">Samples</a> |
| TRS3232EIDW      | LIFEBUY       | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | TRS3232EI               |                         |
| TRS3232EIPWR     | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | RS32EI                  | <a href="#">Samples</a> |
| TRS3232EIPWRG4   | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | RS32EI                  | <a href="#">Samples</a> |
| TRS3232EIRGTR    | ACTIVE        | VQFN         | RGT                | 16   | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 3232                    | <a href="#">Samples</a> |
| TRSF3232ECDWR    | LIFEBUY       | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | TRSF3232EC              |                         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TRS3232E :**

- Automotive : [TRS3232E-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRS3232ECDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TRS3232ECDWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| TRS3232ECPWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TRS3232ECPWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TRS3232EIDBR  | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| TRS3232EIDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TRS3232EIPWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TRS3232EIPWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TRS3232EIRGTR | VQFN         | RGT             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TRSF3232ECDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRS3232ECDR   | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| TRS3232ECDWR  | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| TRS3232ECPWR  | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| TRS3232ECPWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| TRS3232EIDBR  | SSOP         | DB              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| TRS3232EIDR   | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| TRS3232EIPWR  | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| TRS3232EIPWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| TRS3232EIRGTR | VQFN         | RGT             | 16   | 3000 | 367.0       | 367.0      | 35.0        |
| TRSF3232ECDWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |

## TUBE



\*All dimensions are nominal

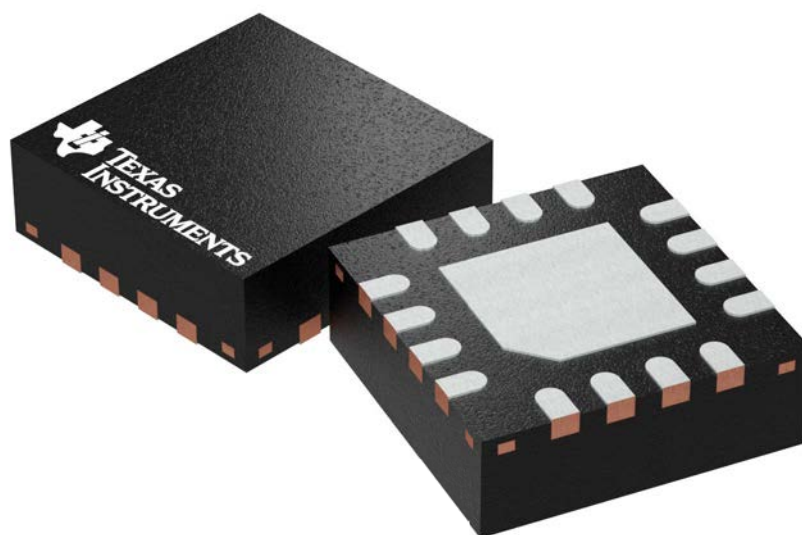
| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TRS3232ECDW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| TRS3232EIDW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |

**RGT 16**

**GENERIC PACKAGE VIEW**

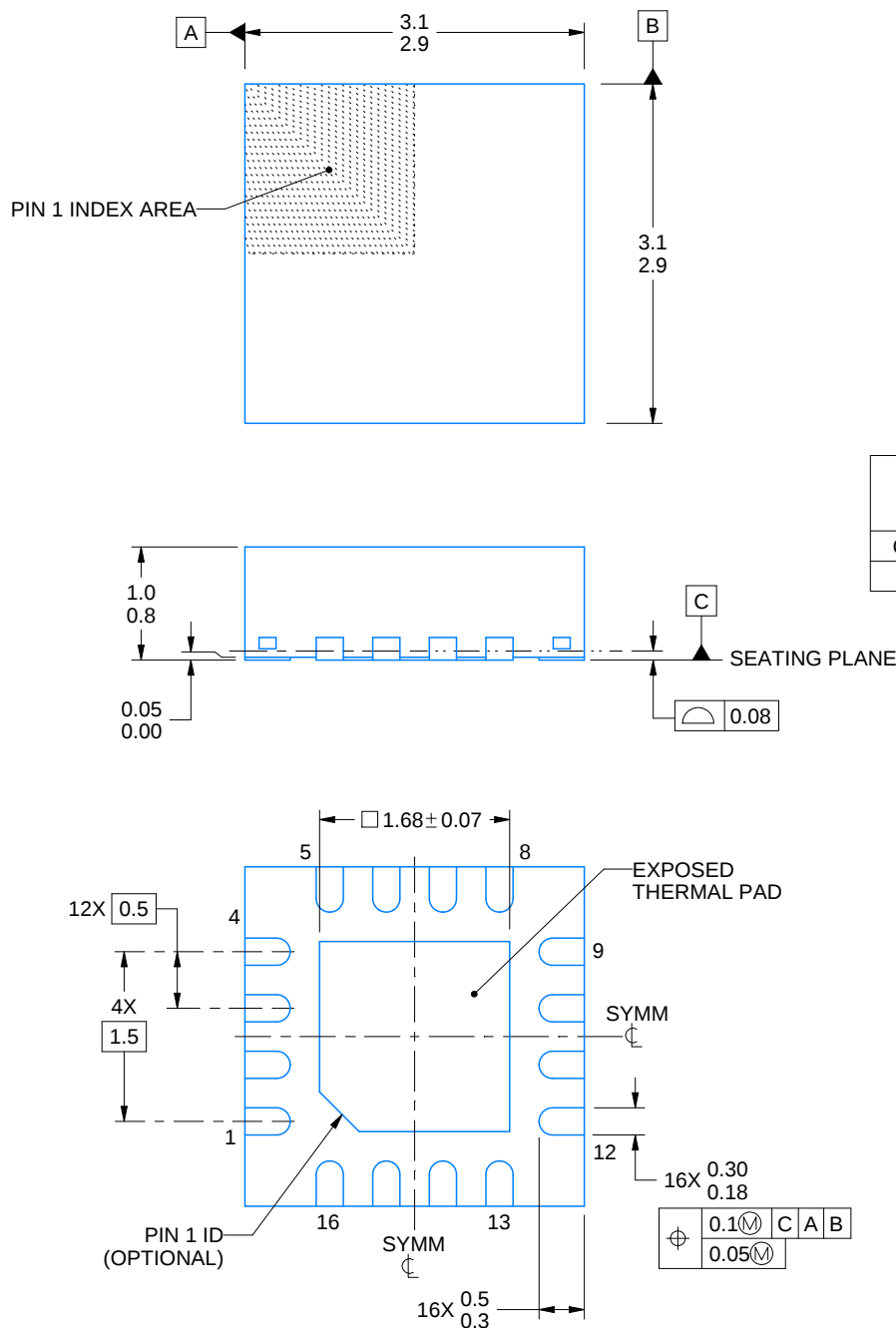
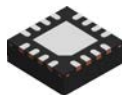
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



4222419/D 04/2022

## NOTES:

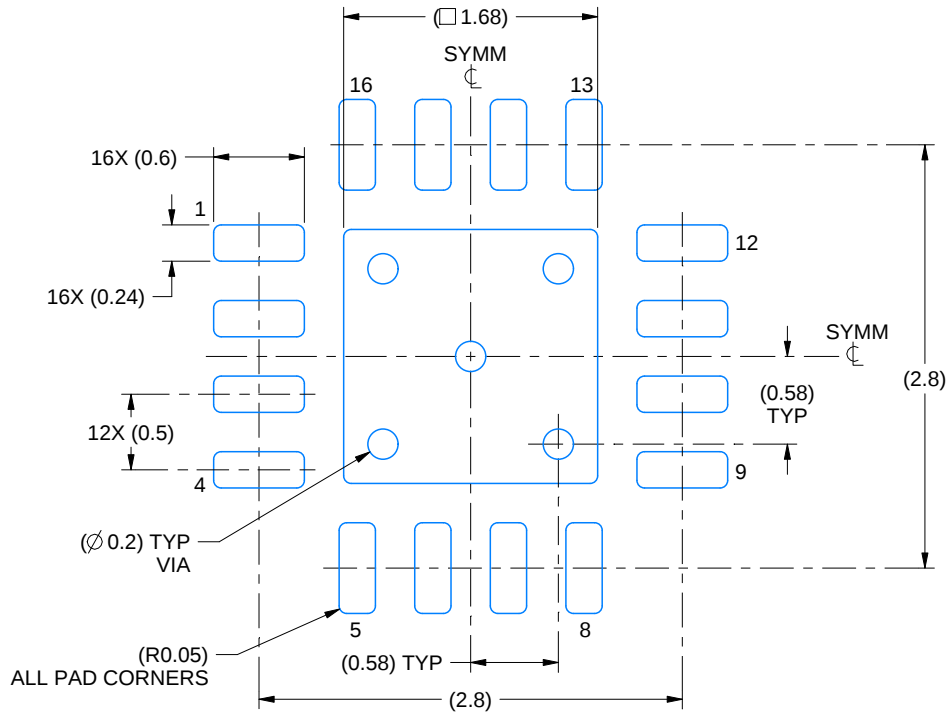
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

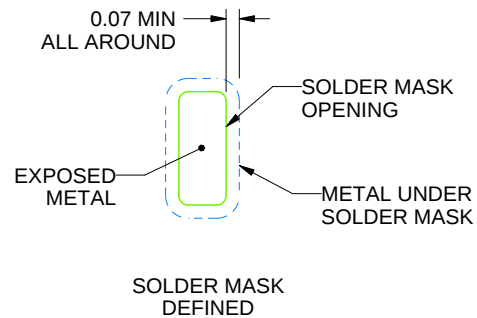
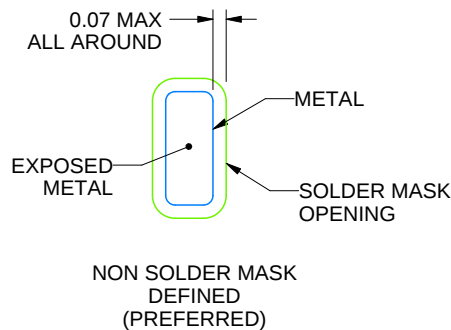
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

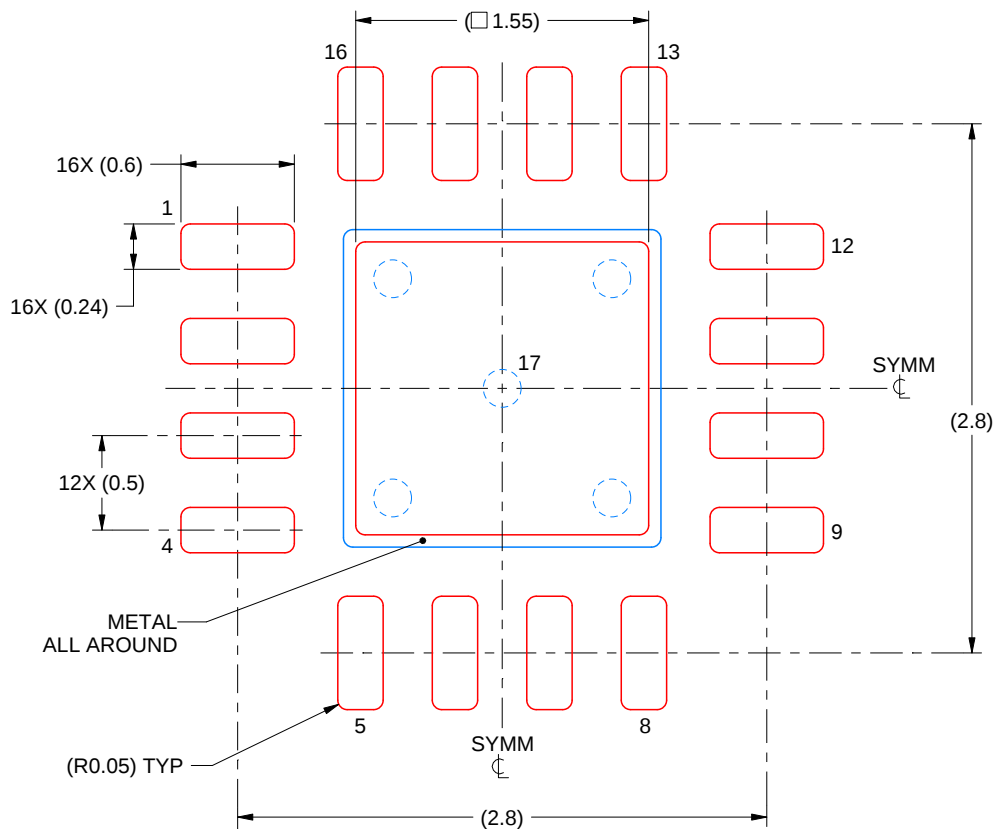
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

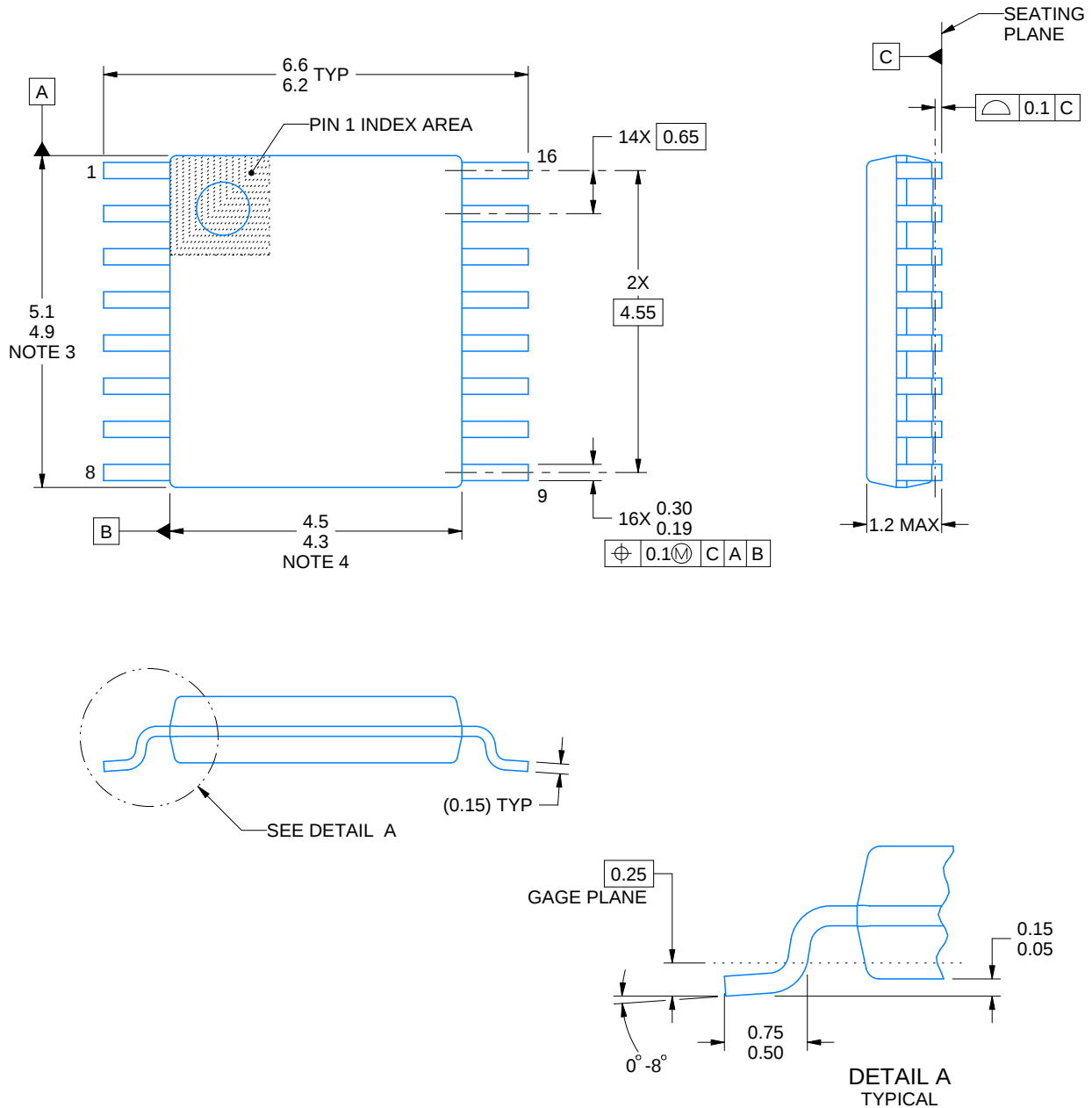
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

## NOTES:

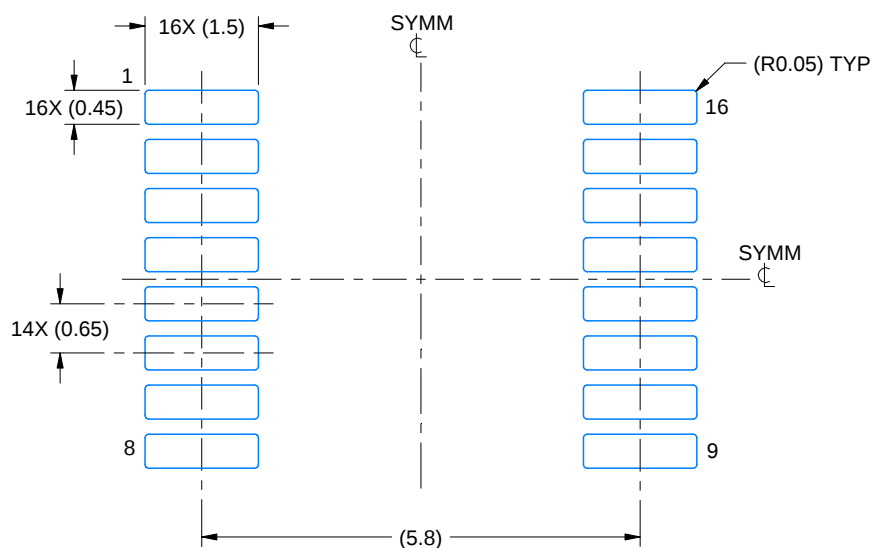
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

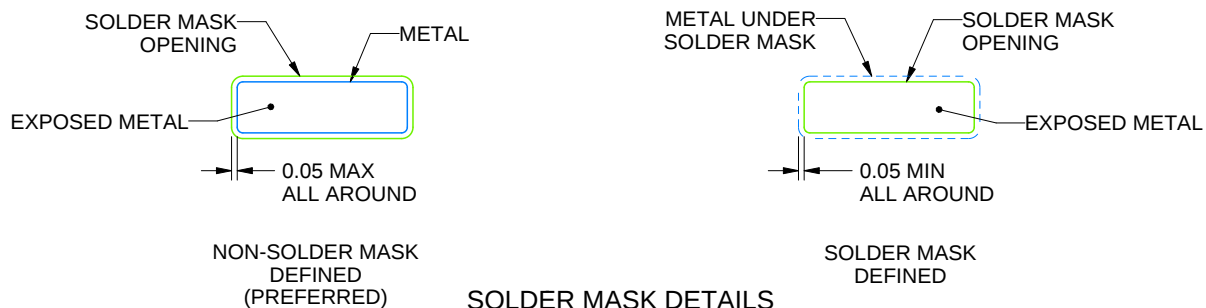
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

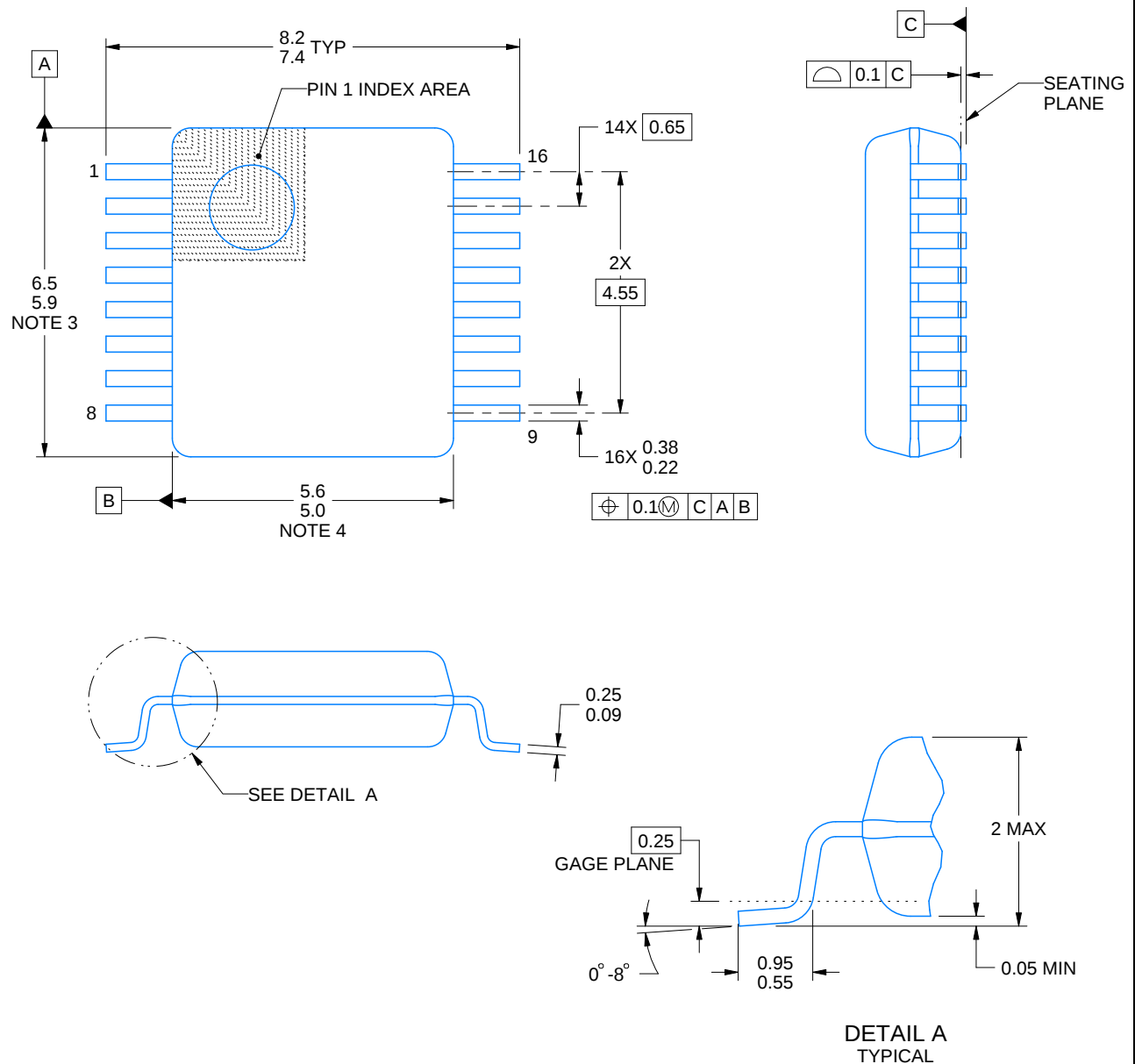


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220763/A 05/2022

## NOTES:

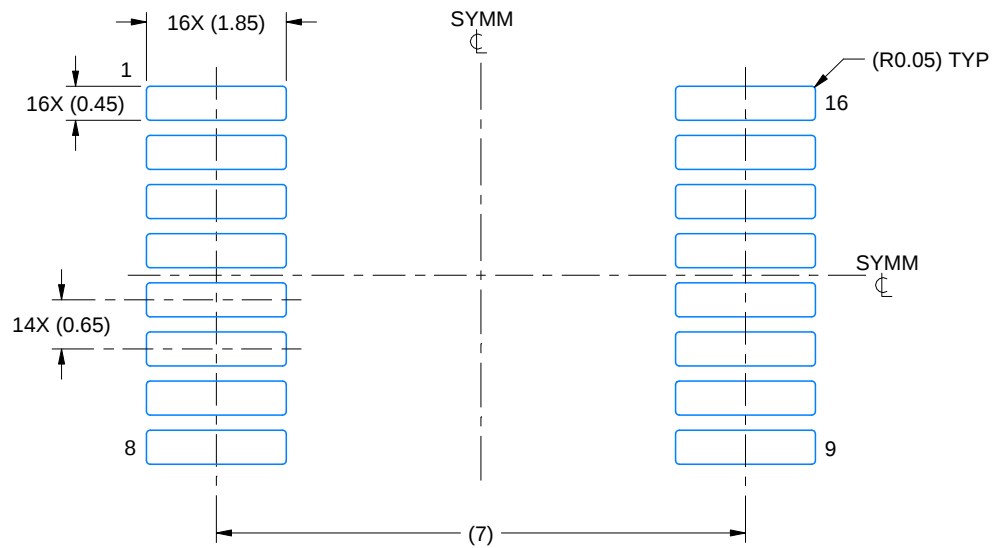
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

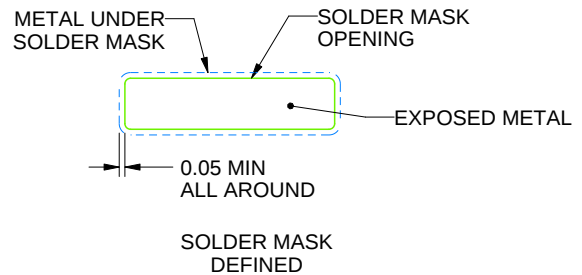
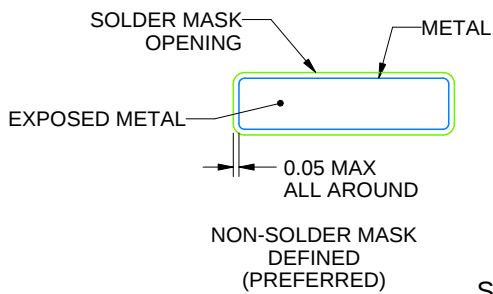
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

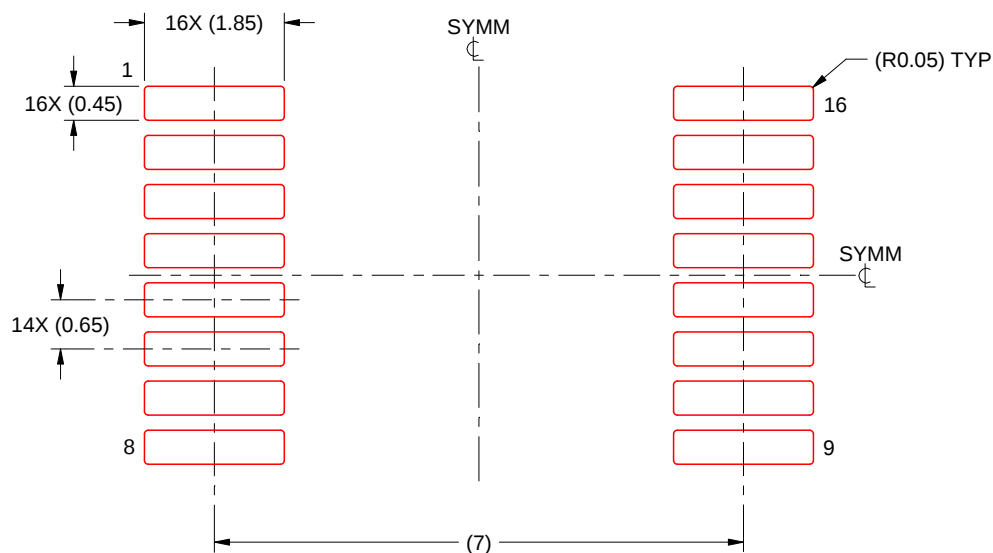
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

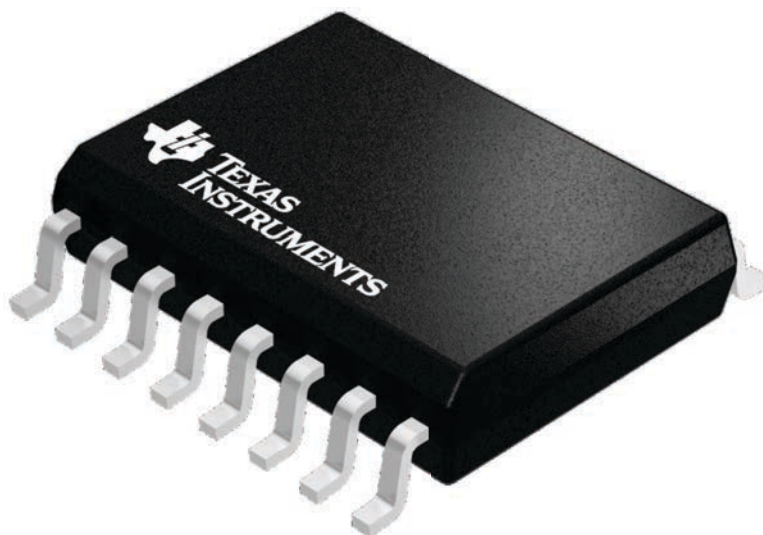
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

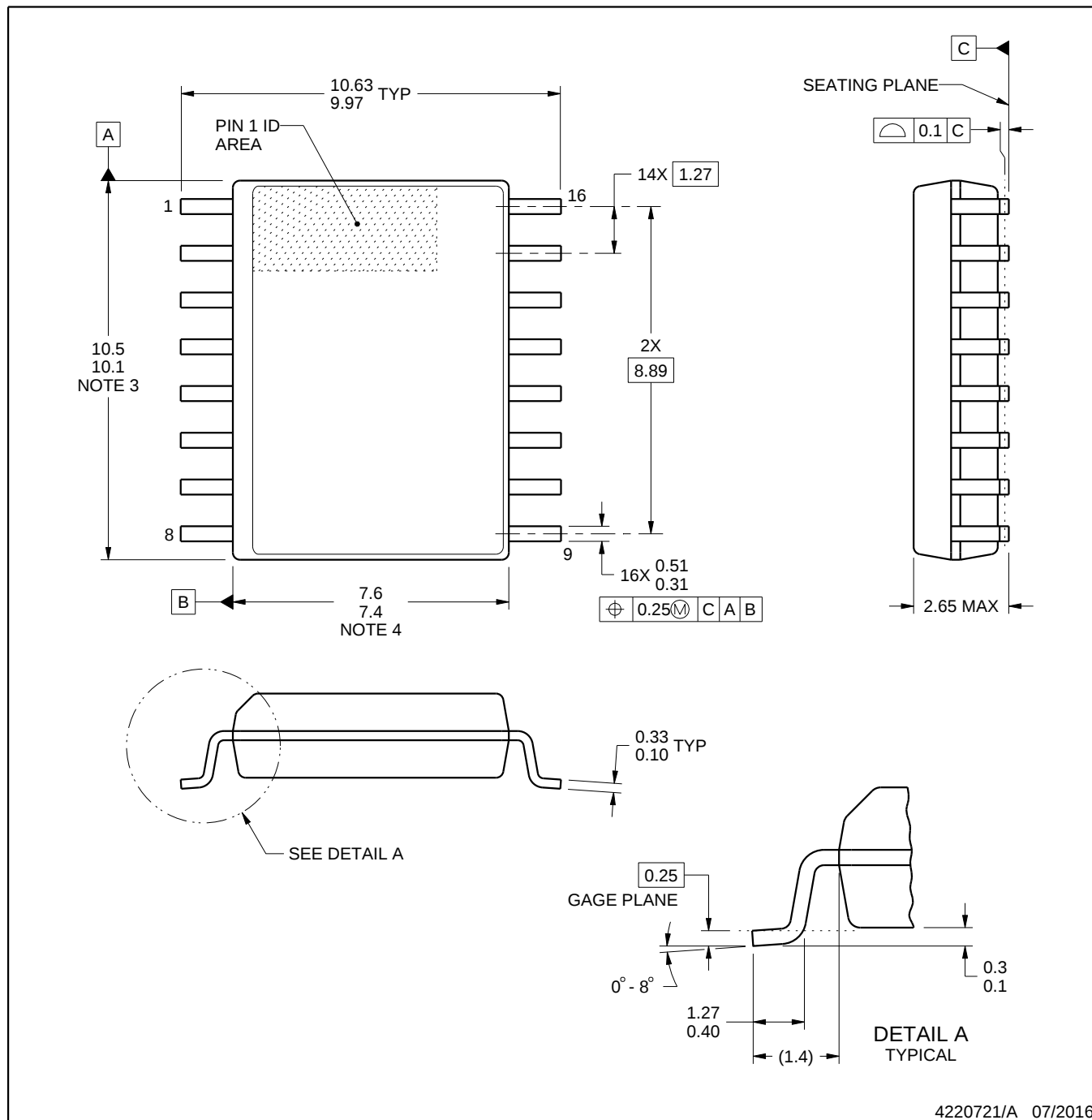


DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

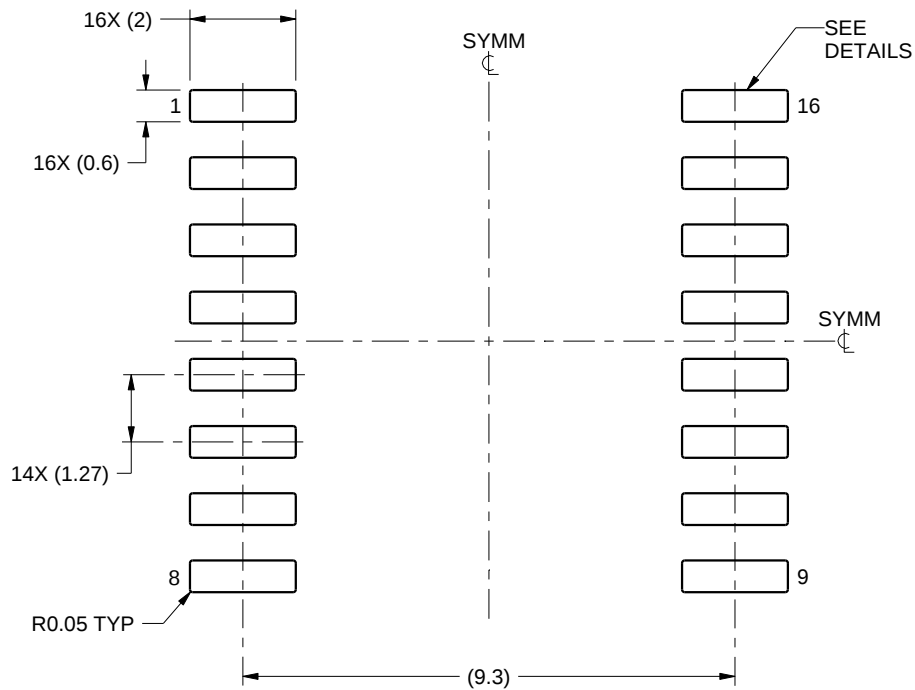
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

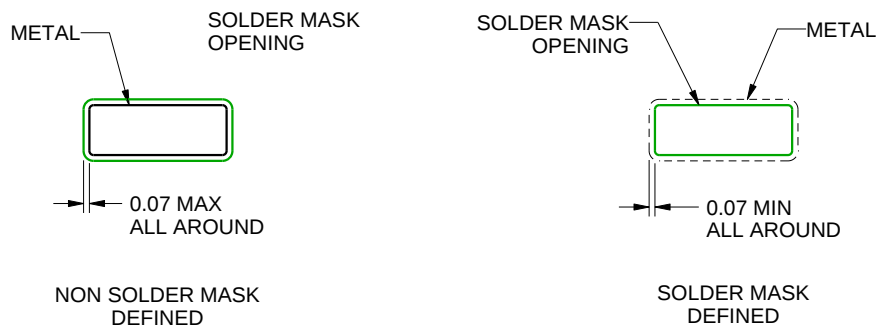
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

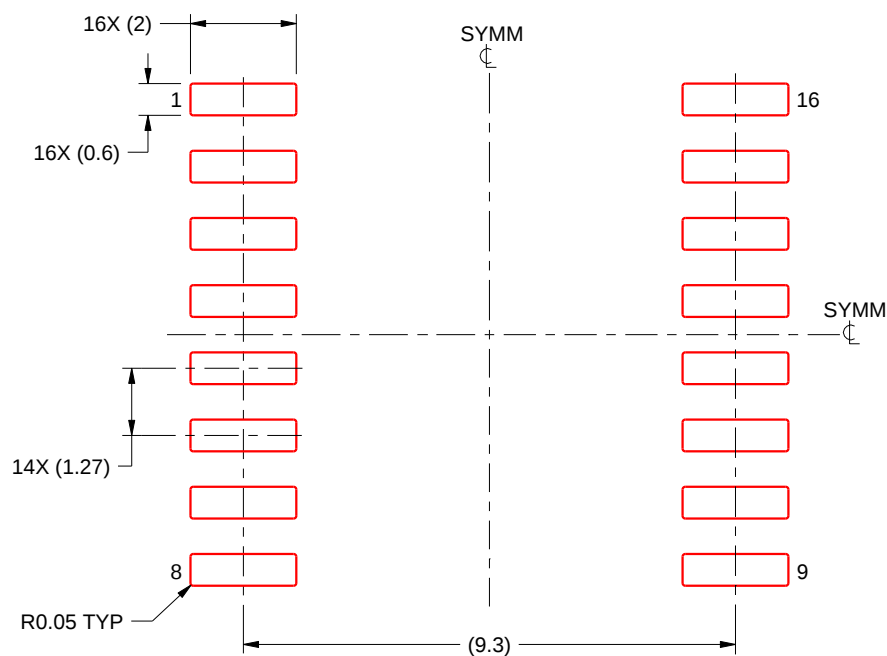
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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