SNx5HVD1176 PROFIBUS® RS-485 收发器

1 特性

- 针对 PROFIBUS® 网络进行了优化
  - 信号传输速率高达 40Mbps
  - 差分输出超过 2.1V（54Ω 负载）
  - 10pF（最大值）的低总线电容
- 符合 TIA/EIA-485-A 的要求
- ESD 保护超过 ±10kV HBM
- 针对总线开路、短路及空闲状态的失效防护接收器
- 一条总线上多达 160 个收发器
- 输出转换以及驱动器启用和禁用期间的低偏斜
- 共模抑制高达 50MHz
- 短路电流限制
- 支持热插拔
- 热关断保护

2 应用

- 过程自动化
  - 化学品生产
  - 酿造和蒸馏
  - 造纸机
- 工厂自动化
  - 汽车生产
  - 滚动机、压印机、冲压机
  - 联网传感器
- 通用 RS-485 网络
  - 电机和运动控制
  - HVAC 及楼宇自动化网络
  - 联网安检站

3 说明

SNx5HVD1176 器件是半双工差分收发器，其特性针对 PROFIBUS (EN 50170) 应用进行了优化。在 54Ω 负载下，驱动器输出差分电压超过了 PROFIBUS 要求的 2.1V。具有高达 40Mbps 的信号传输速率，能够在技术上实现高数据传输速度。低总线电容可提供低信号失真。

SN65HVD1176 和 SN75HVD1176 器件符合或超过 ANSI 标准 TIA/EIA-485-A (RS-485) 的要求，适用于双绞线网络上的差分数据传输。驱动器输出端和接收器输入端连接在一起，形成一个具有五分之一单位负载的半双工总线端口，从而在单路总线上支持多达 160 个节点。当总线短路、保持开路或没有驱动器处于活动状态时，接收器输出保持在逻辑高电平。当电源电压低于 2.5V 时，驱动器输出处于高阻抗状态，以防止电源循环期间或带电插入总线期间产生总线干扰。内部电流限制可将输出电流限制为恒定值，从而在短路故障条件下保护收发器总线引脚。热关断电路可保护器件免受因负载和驱动条件而导致的功率耗散过大所造成的损坏。

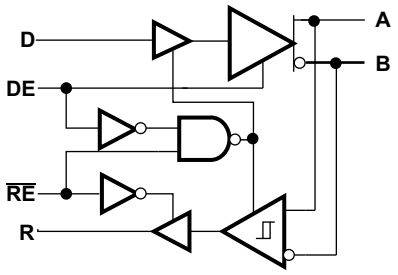
SN75HVD1176 器件的额定工作温度范围为 0°C 至 70°C。SN65HVD1176 器件的额定工作温度范围为 –40°C 至 85°C。

有关此器件的分离式版本，请参阅具有集成数字隔离器的 ISO1176 器件 (SLLS897)。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
SN65HVD1176 SN75HVD1176	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

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4 Revision History

Changes from Revision H (September 2015) to Revision I (January 2023) **Page**

- Changed the *Thermal Information* table 5
- Changed the *Typical Characteristics* graphs 10

Changes from Revision G (June 2015) to Revision H (September 2015) **Page**

- Changed V_{ID} ≥ 0.02 V To: V_{ID} ≥ –0.02 V in 表 7-2 17

Changes from Revision F (June 2013) to Revision G (June 2015) **Page**

- 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*功率损耗* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 1
- Added storage temperature to the *Absolute Maximum Ratings* table 4
- Added Psi JT and Psi JB values to the *Thermal Information* table 5
- Deleted redundant $I_{O(OFF)}$ and I_{OZ} lines from the *Electrical Characteristics* table 6
- Deleted redundant C_{OD} line from the *Electrical Characteristics* table 6

Changes from Revision E (August 2008) to Revision F (June 2013) **Page**

- 将引脚分配和逻辑图中的 RE 更改为 $\overline{RE}$ 1

5 Pin Configuration and Functions

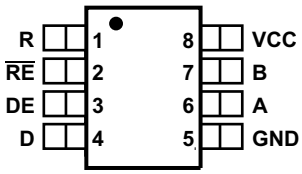


图 5-1. D Package 8-Pin SOIC Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output/receiver input (complementary to B)
B	7	Bus input/output	Driver output/receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable low
VCC	8	Supply	3-V to 5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	7	V
	Voltage at any bus I/O terminal	–9	14	V
	Voltage input, transient pulse, A and B, (through 100 Ω, see 图 7-15)	–40	40	V
	Voltage input at any D, DE or $\overline{RE}$ terminal	–0.5	7	V
I_O	Receiver output current	–10	10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–40	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
			Bus terminals and GND	±10000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IL}	Differential input voltage	A with respect to B	–12		12	V
I_O	Output current	Driver	–70		70	mA
		Receiver	–8		8	mA
T_J	Junction temperature (1)	SN65HVD1176	–40		130	°C
		SN75HVD1176	0		130	°C
R_L	Differential load resistance		54			Ω
$1/t_{U1}$	Signaling rate				40	Mbps

(1) See the 节 6.7 table for more information on maintenance of this requirement.

6.4 Thermal Information

THERMAL METRIC(1)		SN75HVD1176 D (SOIC) 8 PINS	SN65HVD1176 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	104.7	116.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.9	63.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.7	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.2	62.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The intent of $R_{\theta JA}$ specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER							
V_O	Open-circuit output voltage	A or B	No load	0		V_{CC}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude	R_L = 54 Ω	See 图 7-1	2.1	2.9		V
		With common-mode loading, (V_{TEST} from – 7 V to 12 V) See 图 7-2		2.1	2.7		V
$\Delta\|V_{OD(SS)}\|$	Change in steady-state differential output voltage between logic states	See 图 7-1 and 图 7-6		– 0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 7-5		2	2.5	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See 图 7-5		– 0.2	0	0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See 图 7-5			0.5		V
$V_{OD(RING)}$	Differential output voltage over and under shoot	R_L = 54 Ω, C_L = 50 pF See 图 7-6				10%	$V_{OD(PP)}$
I_I	Input current	D, DE		– 50		50	μA
$I_{OS(P)}$	Peak short-circuit output current	DE at V_{CC}, See 图 7-8	V_{OS} = – 7 V to 12 V	– 250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current	DE at V_{CC}, See 图 7-8	V_{OS} > 4 V, Output driving low	60	90	135	mA
			VOS < 1 V, Output driving high	– 135	– 90	– 60	mA
RECEIVER							
$V_{IT(+)}$	Positive-going differential input voltage threshold	See 图 7-9	V_O = 2.4 V, I_O = – 8 mA		– 80	– 20	mV
$V_{IT(-)}$	Negative-going differential input voltage threshold		V_O = 0.4 V, I_O = 8 mA	– 200	– 120		mV
V_{HYS}	Hysteresis voltage (V_{IT+} – V_{IT-})				40		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = – 8 mA, See 图 7-9		4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = – 200 mV, I_{OL} = 8 mA, See 图 7-9			0.2	0.4	V
I_A, I_B	Bus pin input current	V_I = – 7 V to 12 V, Other input = 0 V	V_{CC} = 4.75 V to 5.25 V	– 160		200	μA
$I_{A(OFF)}$ $I_{B(OFF)}$			V_{CC} = 0 V	– 160		200	
I_I	Receiver enable input current	$\overline{RE}$		– 50		50	μA
I_{OZ}	High-impedance - state output current	$\overline{RE}$ = V_{CC}		– 1		1	μA
R_I	Input resistance			60			kΩ
C_{ID}	Differential input capacitance	Test input signal is a 1.5-MHz sine wave with amplitude 1 V_{PP}, capacitance measured across A and B			7	10	pF
C_{MR}	Common mode rejection	See 图 7-11			4		V

(1) All typical values are at V_{CC} = 5 V and 25°C.

6.6 Supply Current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply Current(1)	Driver and receiver, $\overline{RE}$ at 0 V, DE at V_{CC}, All other inputs open, no load		4	6	mA
		Driver only, $\overline{RE}$ at V_{CC}, DE at V_{CC}, All other inputs open, no load		3.8	6	mA
		Receiver only, $\overline{RE}$ at 0 V, DE at 0 V, All other inputs open, no load		3.6	6	mA
		Standby only, $\overline{RE}$ at V_{CC}, DE at 0 V, All other inputs open		0.2	5	μA

(1) Over recommended operating conditions

6.7 Power Dissipation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
P_D	Device power dissipation		R_L = 54 Ω, C_L = 50 pF, 0 V to 3 V, 15 MHz, 50% duty cycle square wave input, driver and receiver enabled		277	318	mW
T_A	Ambient air temperature	SN65HVD1176	Low-K board, no air flow, P_D = 318 mW	–40		64	°C
			High-K board, no air flow, P_D = 318 mW	–40		89	°C
		SN75HVD1176	Low-K board, no air flow, P_D = 318 mW	0			°C
			High-K board, no air flow, P_D = 318 mW	0			°C
T_{SD}	Thermal shut down junction temperature				150		°C

(1) All typical values are with V_{CC} = 5 V and T_A = 25°C.

6.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER							
t_{PLH}	Propagation delay time low-level-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See 图 7-3		4	7	10	ns
t_{PHL}	Propagation delay time high-level-to-low-level output			4	7	10	ns
$t_{sk(p)}$	Pulse skew | t_{PLH} – t_{PHL} |				0	2	ns
t_r	Differential output rise time			2	3	7.5	ns
t_f	Differential output fall time			2	3	7.5	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew	See 图 7-4			0.2	1	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output	R_L = 110 Ω, C_L = 50 pF See 图 7-7	$\overline{RE}$ at 0 V		10	20	ns
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-to- high-impedance output				10	20	ns
$\lvert t_{p(AZL)} - t_{p(BZH)} \rvert$ $\lvert t_{p(AZH)} - t_{p(BZL)} \rvert$	Enable skew time				0.55	1.5	ns
$\lvert t_{p(ALZ)} - t_{p(BHZ)} \rvert$ $\lvert t_{p(AHZ)} - t_{p(BLZ)} \rvert$	Disable skew time					2.5	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output (from sleep mode)	R_L = 110 Ω, C_L = 50 pF See 图 7-7	$\overline{RE}$ at 5 V		1	4	μs
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-output-to high-impedance (to sleep mode)				30	50	ns

6.8 Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{(CFB)}$	Time from application of short-circuit to current foldback	See 图 7-8		0.5		µs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown	T_A = 25°C, See 图 7-8	100			µs

6.8 Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
RECEIVER						
t_{PLH}	Propagation delay time, low-to-high level output	See 图 7-10		20	25	ns
t_{PHL}	Propagation delay time, high-to-low level output			20	25	ns
$t_{sk(p)}$	Pulse skew | t_{PLH} – t_{PHL} |			1	2	ns
t_r	Receiver output voltage rise time			2	4	ns
t_f	Receiver output voltage fall time			2	4	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	DE at V_{CC}, See 图 7-13			20	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	DE at V_{CC}, See 图 7-14			20	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				20	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output (standby to active)	DE at 0 V, See 图 7-12		1	4	μs
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output (active to standby)			13	20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output (standby to active)	DE at 0 V, See 图 7-12		2	4	μs
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output (active to standby)			13	20	ns

(1) All typical values are at V_{CC} = 5 V and 25°C.

6.9 Typical Characteristics

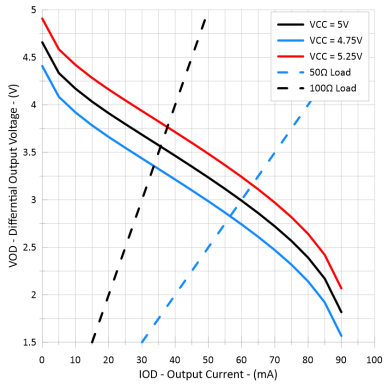


图 6-1. Differential Output Voltage vs Load Current

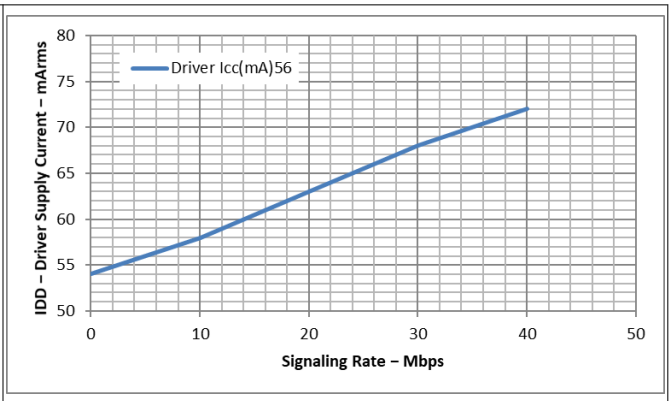


图 6-2. Driver Supply Current vs Signaling Rate

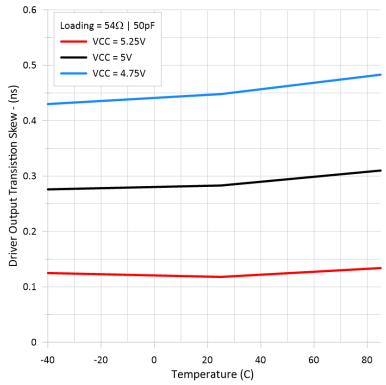


图 6-3. Driver Output Transition Skew vs Free-Air Temperature

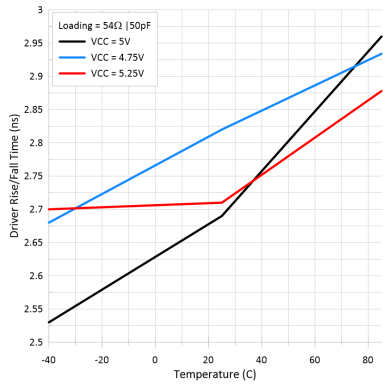


图 6-4. Driver Rise, Fall Time vs Free-Air Temperature

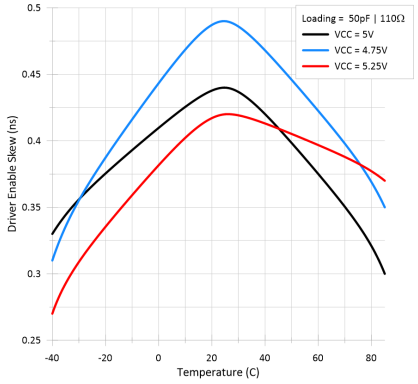


图 6-5. Driver Enable Skew vs Free-Air Temperature

Parameter Measurement Information

备注

Test load capacitance includes probe and jig capacitance (unless otherwise specified).

Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle, Z_o = 50 Ω (unless otherwise specified).

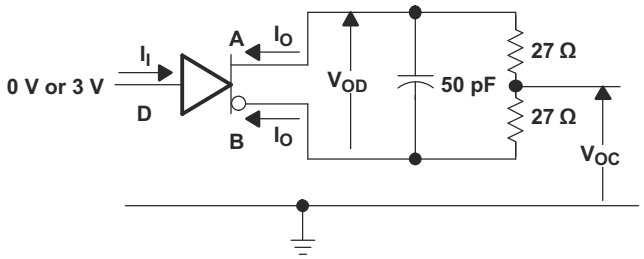


图 7-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

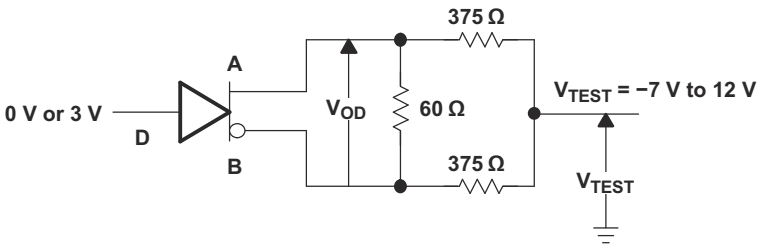


图 7-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

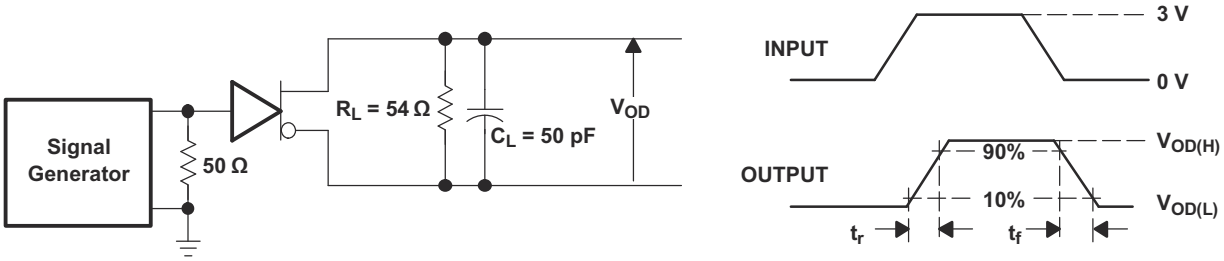


图 7-3. Driver Switching Test Circuit and Rise/Fall Time Measurement

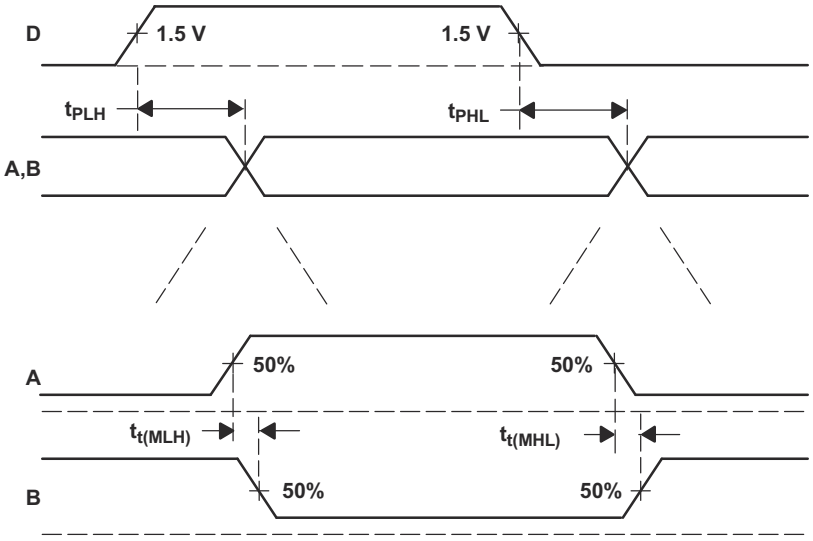


图 7-4. Driver Switching Waveforms for Propagation Delay and Output Midpoint Time Measurements

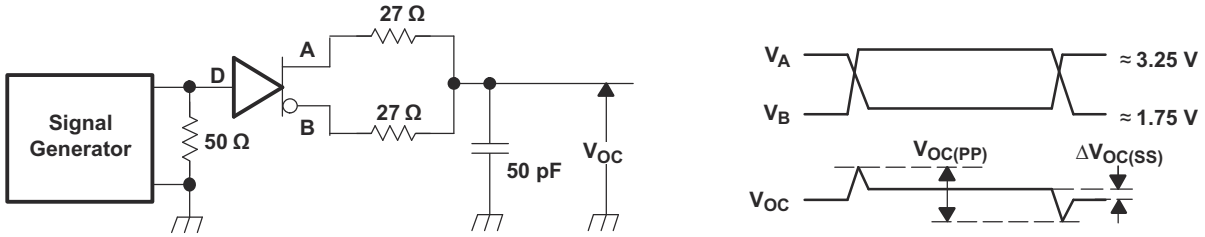
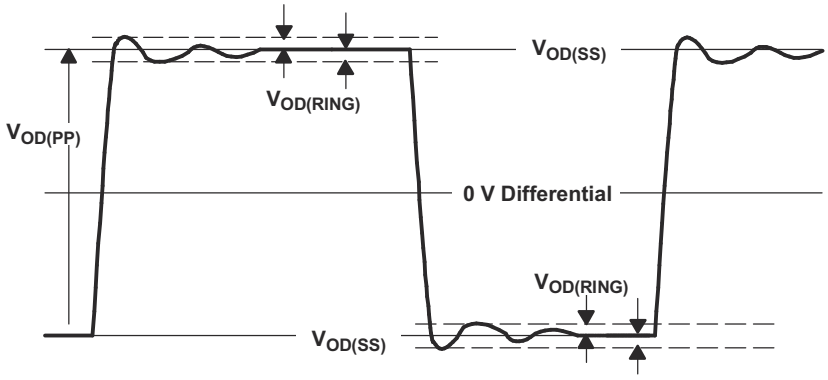


图 7-5. Driver V_{OC} Test Circuit and Waveforms



A. $V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

图 7-6. $V_{OD(RING)}$ Waveform and Definitions

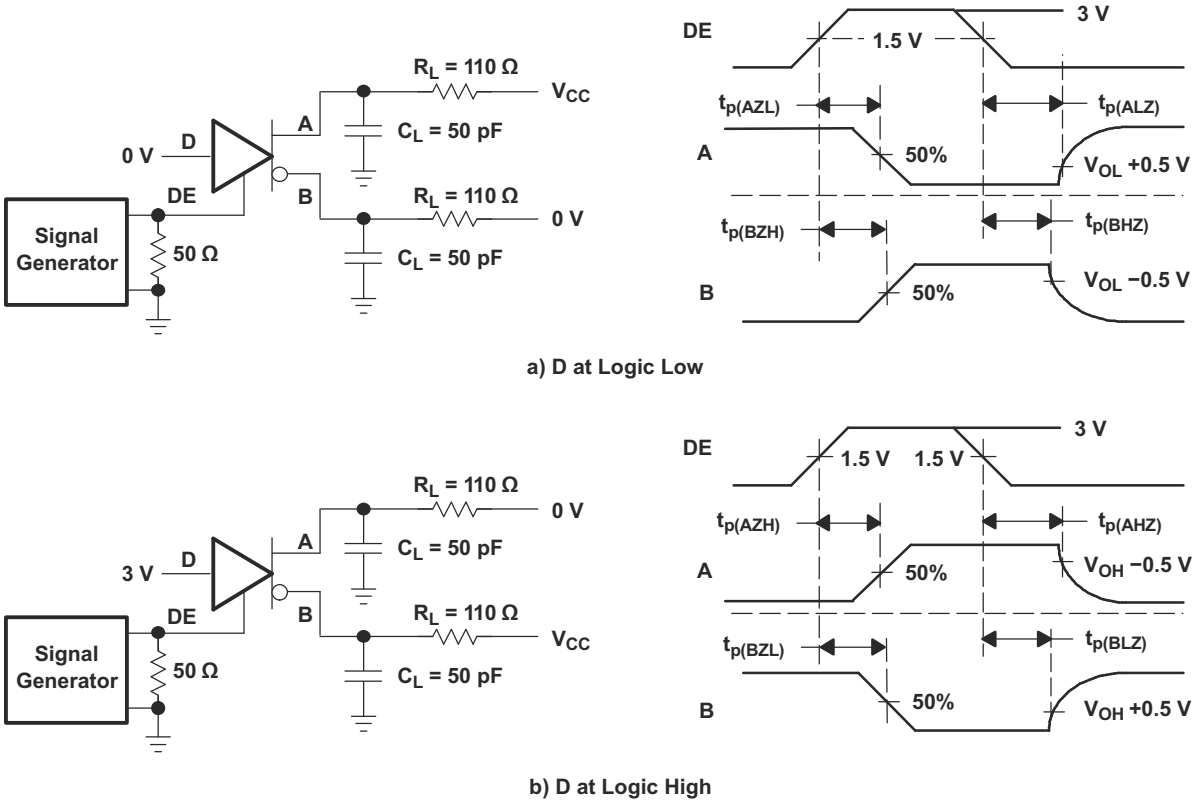


图 7-7. Driver Enable/Disable Test

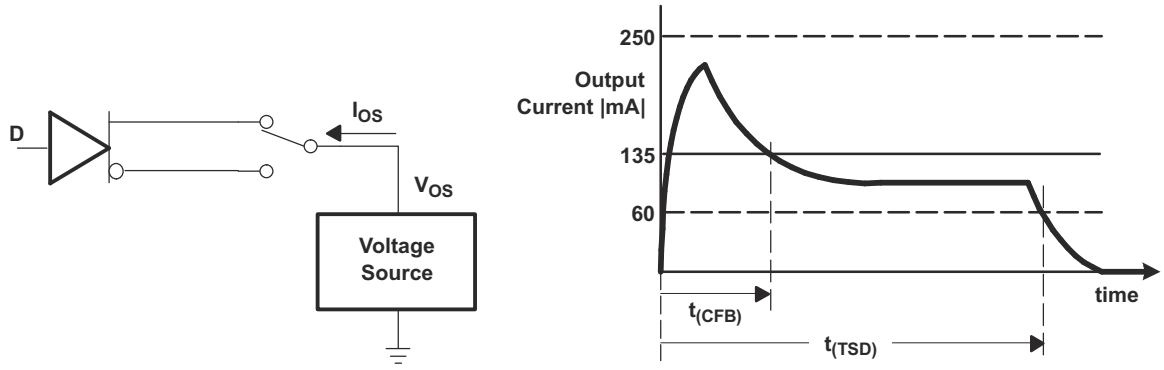


图 7-8. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t = 0)

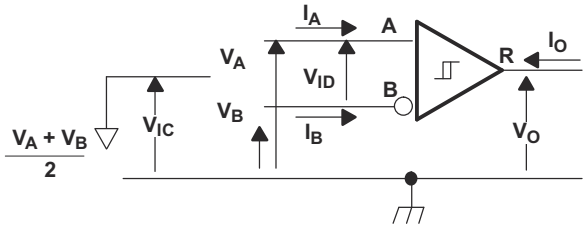


图 7-9. Receiver DC Parameter Definitions

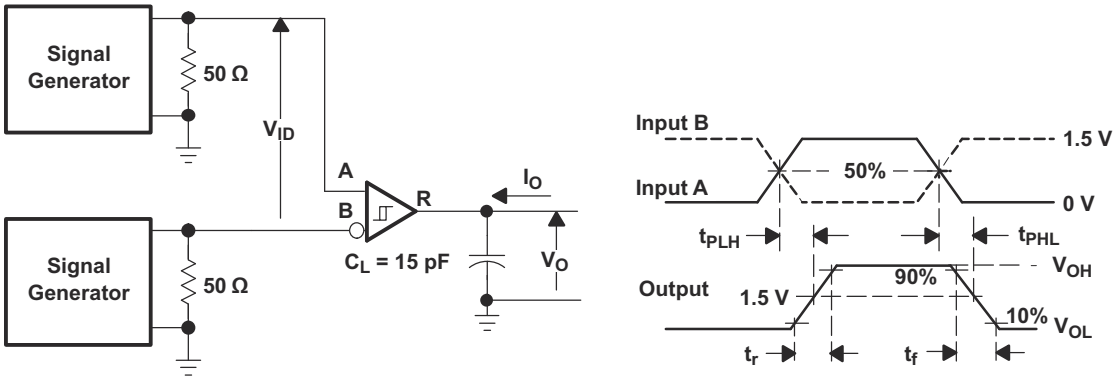


图 7-10. Receiver Switching Test Circuit and Waveforms

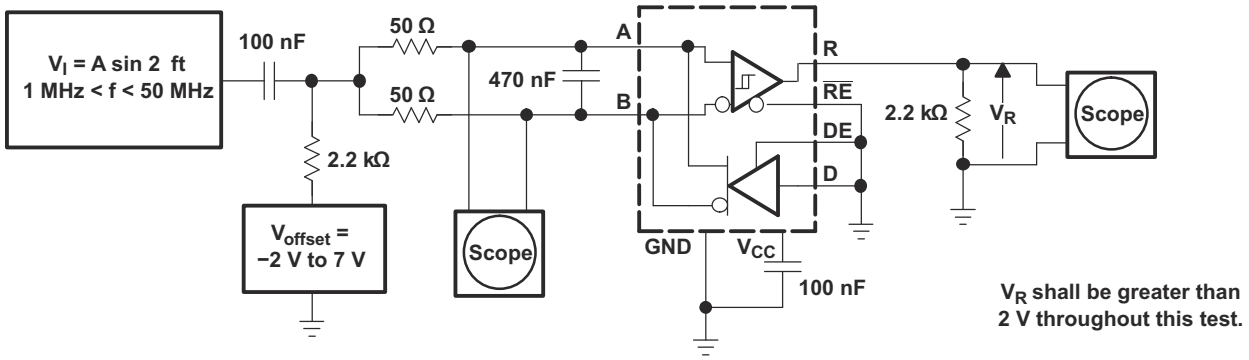


图 7-11. Receiver Common-Mode Rejection Test Circuit

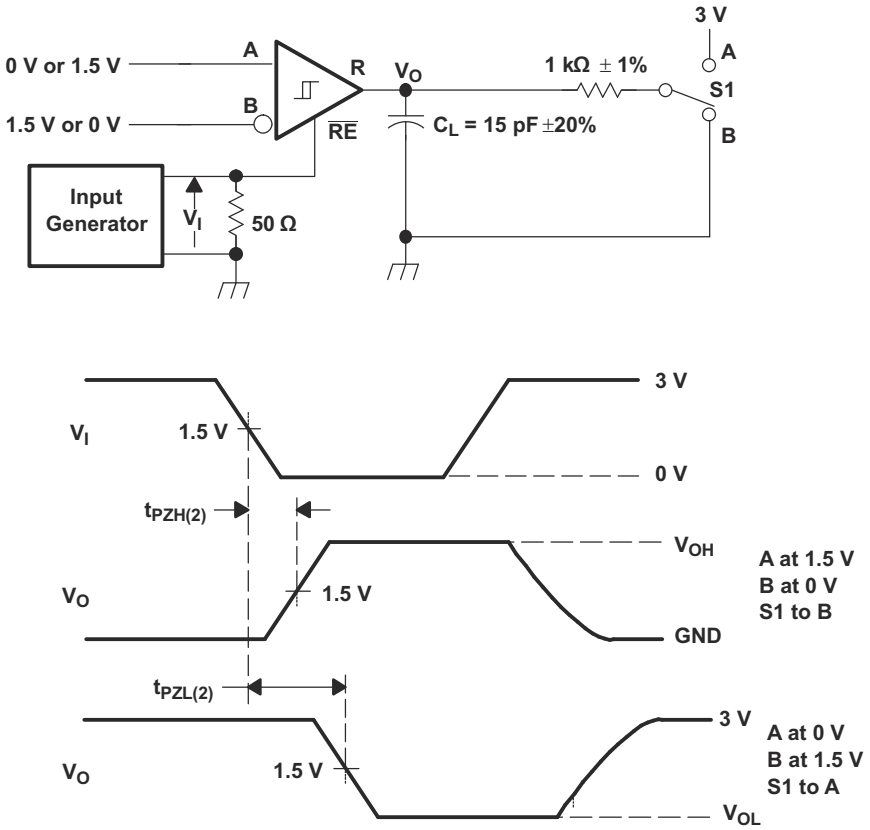


图 7-12. Receiver Enable Time From Standby (Driver Disabled)

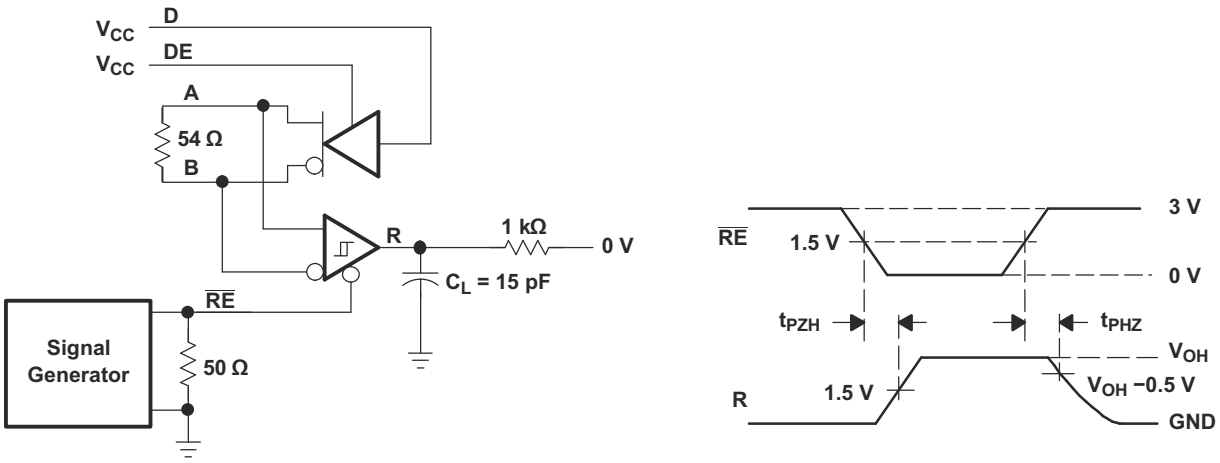


图 7-13. Receiver Enable Test Circuit and Waveforms, Data Output High (Driver Active)

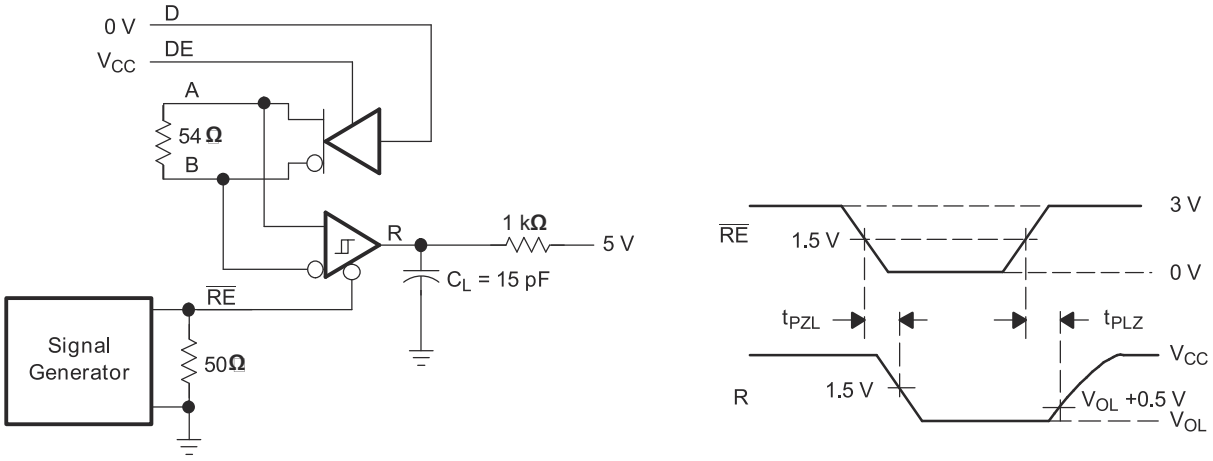


图 7-14. Receiver Enable Test Circuit and Waveforms, Data Output Low (Driver Active)

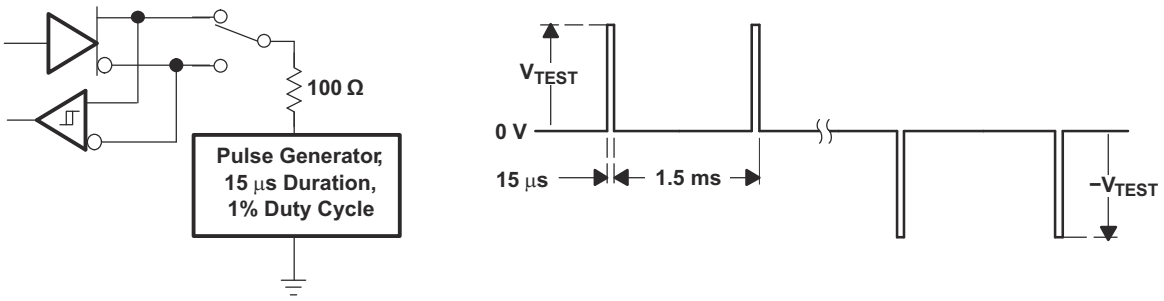


图 7-15. Test Circuit and Waveforms, Transient Overvoltage Test

7 Detailed Description

7.1 Overview

The SNx5HVD1176 device is a 5-V, half-duplex, RS-485 transceiver optimized for use in PROFIBUS (EN50170) applications and suitable for data transmission up to 40 Mbps.

The driver output differential voltage exceeds the PROFIBUS requirement of 2.1 V with a 54-Ω load, and the low transceiver output capacitance of 10 pF supports the PROFIBUS requirements for maximum bus capacitance across various data rates.

This device has an active-high driver enable and an active-low receiver enable. A standby current of less than 5 µA can be achieved by disabling both driver and receiver.

7.2 Functional Block Diagram

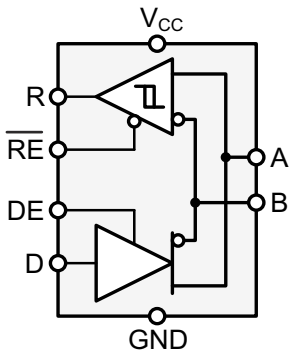


图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±10-kV Human Body Model (HBM) electrostatic discharges and all other pins up to ±4 kV.

The SN65HVD1176 device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions, and a typical receiver hysteresis of 40 mV.

7.4 Device Functional Modes

表 7-1. Driver Function Table(1)

INPUT	ENABLE	OUTPUTS	
D	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	H	L

(1) H = high level, L = low level, X = don’t care,
Z = high impedance (off)

表 7-2. Receiver Function Table(1)

DIFFRENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq -0.02$ V	L	H
-0.2 V < V_{ID} < -0.02 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

表 7-2. Receiver Function Table(1) (continued)

DIFFRENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
X	OPEN	Z
Open Circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = high level, L = low level, X = don’t care,
Z = high impedance (off), ? = indeterminate

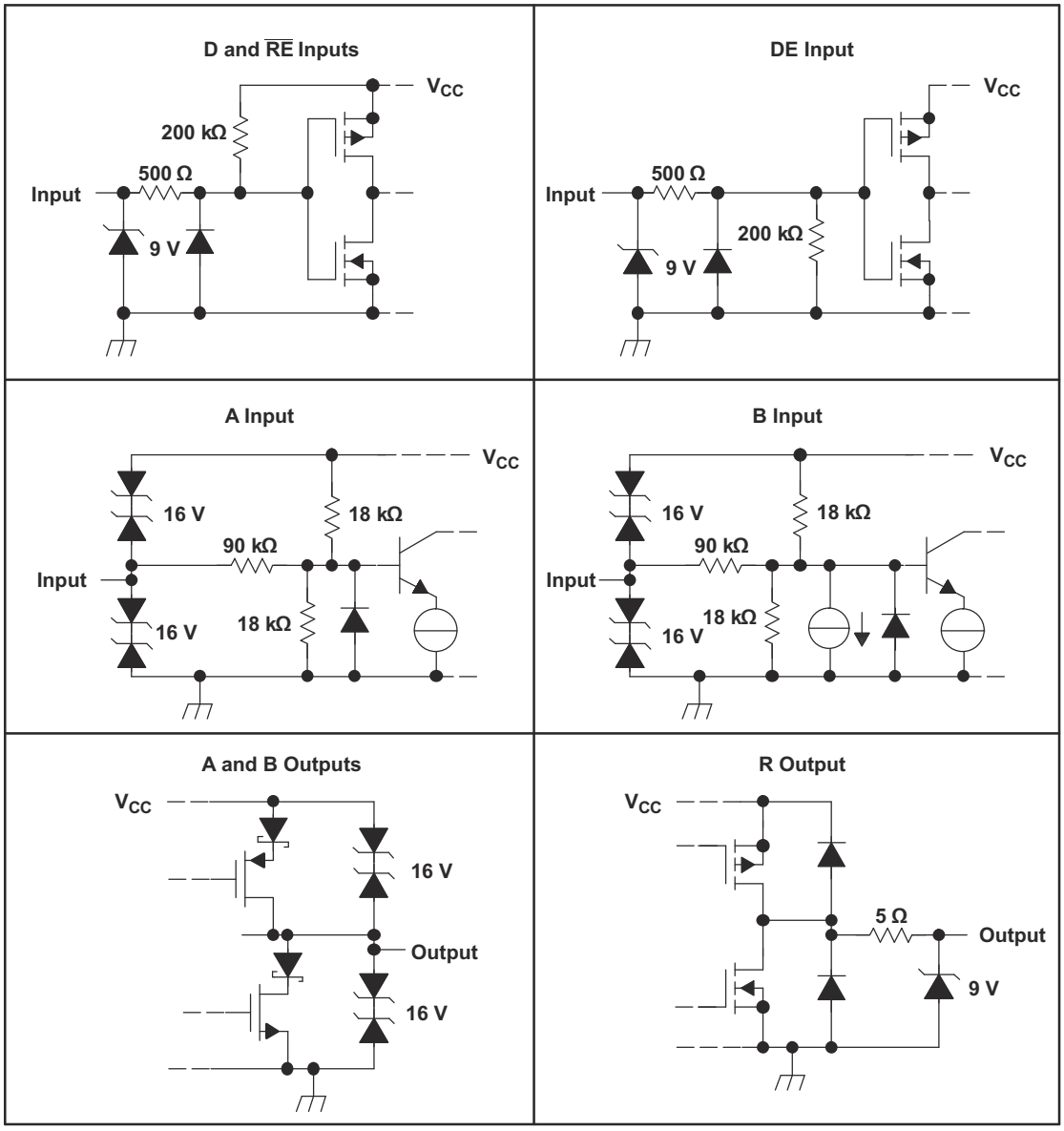


图 7-2. Equivalent Input and Output Schematic Diagrams

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN65HVD1176 device is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver- and receiver-enable pins allow for the configuration of different operating modes.

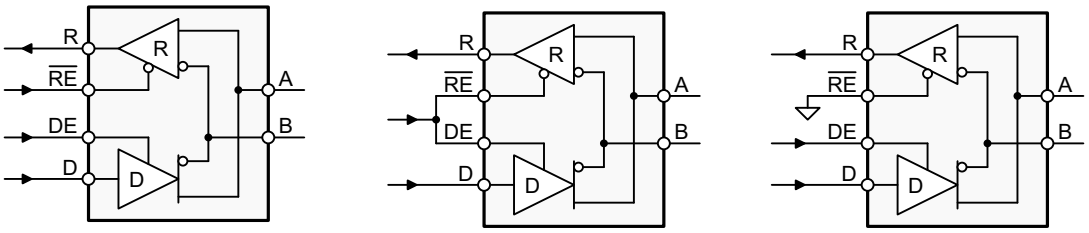


图 8-1. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control because it allows the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node receives the data from the bus and the data it sends; the node can also verify that the correct data has been transmitted.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor (R_T) whose value matches the characteristic impedance (Z_0) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

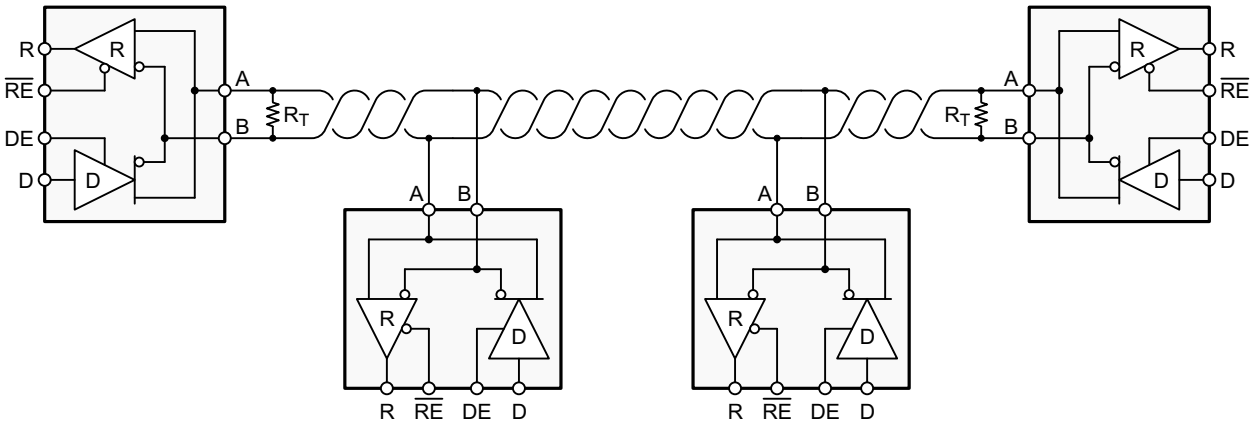


图 8-2. Typical RS-485 Network With Half-Duplex Transceivers

The PROFIBUS standard extends RS-485 by specifying the value of the termination resistor, the characteristic impedance of the bus cable, and the value of fail-safe termination at both ends of the bus.

PROFIBUS requires that 220-Ω termination resistors be placed at both ends of the bus, the bus cable impedance be between 135 Ω and 165 Ω, and that 390-Ω fail-safe resistors be placed on both the A and B lines at both ends of the bus.

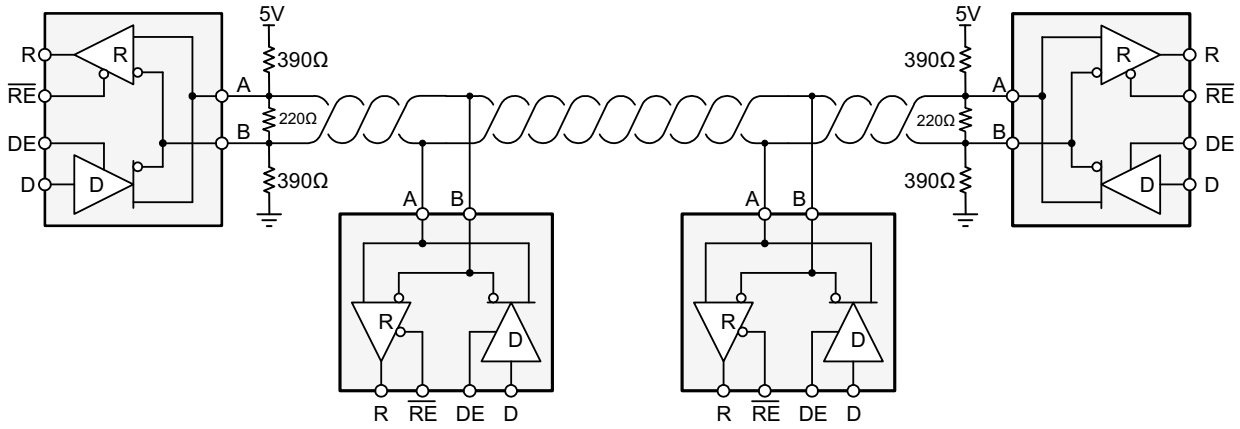


图 8-3. Typical PROFIBUS network

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, that is, the higher the data rate, the shorter the cable length. Conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

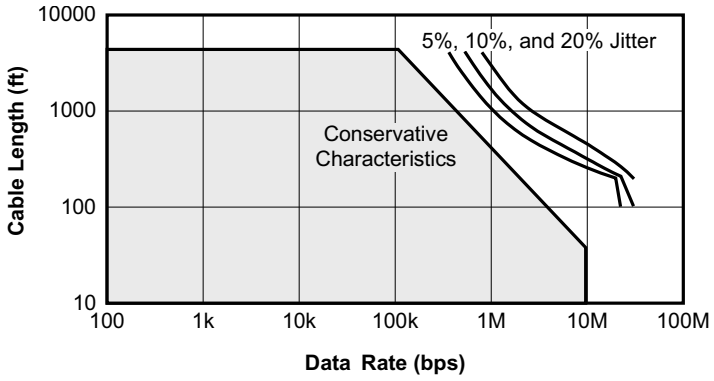


图 8-4. Cable Length vs Data Rate Characteristic

8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 方程式 1.

$$L_{stub} \leqslant 0.1 \times t_r \times v \times c \quad (1)$$

where:

t_r is the 10/90 rise time of the driver
c is the speed of light (3×10^8 m/s)
v is the signal velocity of the cable or trace as a factor of c

Per 方程式 1, the maximum recommended stub length for the minimum driver output rise time of the SN65HVD1176 device for a signal velocity of 78% is 0.05 meters (0.16 feet).

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD1176 device is a 1/5 UL transceiver, it is possible to connect up to 160 receivers to the bus.

8.2.1.4 Receiver Failsafe

The differential receiver of the SN65HVD1176 device is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic-high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input-indeterminate range does not include zero volts differential.

To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input VID is more positive than +200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters that determine the fail-safe performance are $V_{IT(+)}$ and $V_{IT(-)}$.

As shown in 节 6.5, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than –20 mV will always cause a high receiver output. Thus, when the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of –20 mV, and the receiver output will be high.

8.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

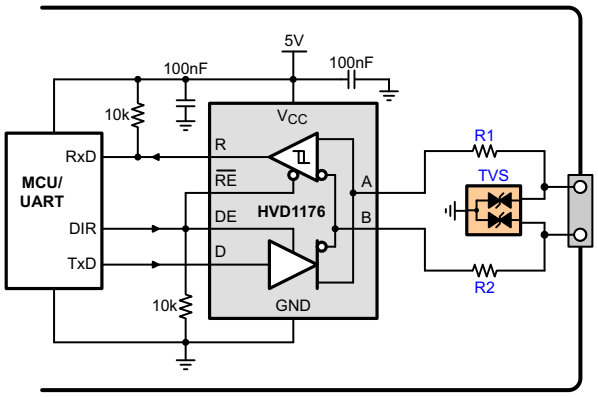


图 8-5. Transient Protection Against ESD, EFT, and Surge Transients

图 8-5 shows a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients. 表 8-1 lists the associated Bill of Materials.

表 8-1. Bill of Materials

Device	Function	Order Number	Manufacturer
XCVR	5-V, 40-Mbps ProfiBus Transceiver	SN65HVD1176	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns

8.2.3 Application Curve

图 8-6 demonstrates operation of the SN65HVD1179 at a signaling rate of 40 Mbps.

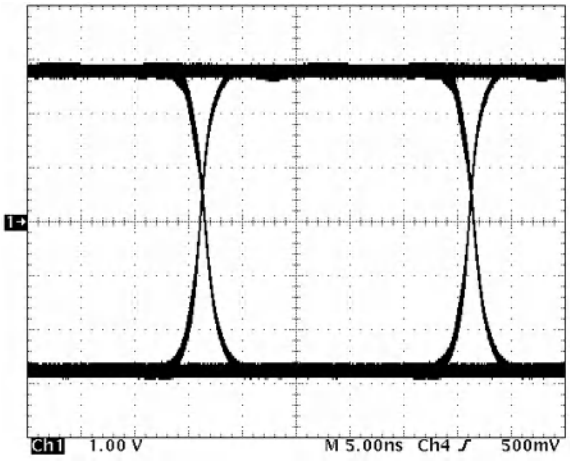


图 8-6. Differential Output of SN65HVD1176 Operation at 40 Mbps

9 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76350 device is a linear voltage regulator suitable for the 5-V supply.

10 Layout

10.1 Layout Guidelines

On-chip IEC-ESD protection is sufficient for laboratory and portable equipment but insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus-node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use VCC and ground planes to provide low-inductance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of the transceiver, the UART, or the controller ICs on the board.
5. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) that reduce the transients to a few hundred volts of clamping voltage and transient blocking units (TBUs) that limit transient current to less than 1 mA.

10.2 Layout Example

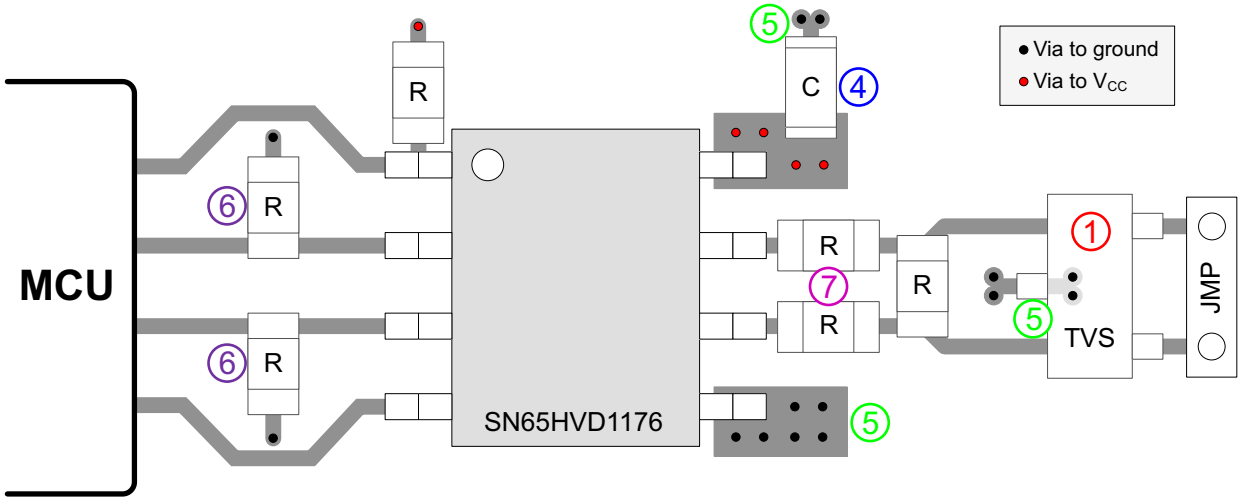


图 10-1. SNx5HVD08 Layout Example

11 Device and Documentation Support

11.1 第三方产品免责声明

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11.2 Documentation Support

For related documentation see the following: *ISO1176 ISOLATED RS-485 PROFIBUS TRANSCEIVER* (SLLS897)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD1176	Click here	Click here	Click here	Click here	Click here
SN75HVD1176	Click here	Click here	Click here	Click here	Click here

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1176D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176	
SN65HVD1176DG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176	
SN65HVD1176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176	Samples
SN65HVD1176DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176	Samples
SN75HVD1176D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN1176	
SN75HVD1176DR	NRND	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN1176	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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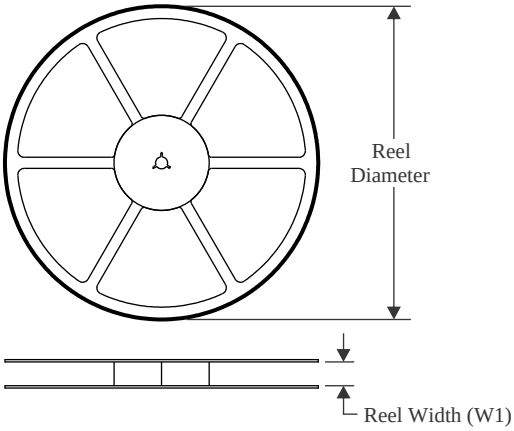
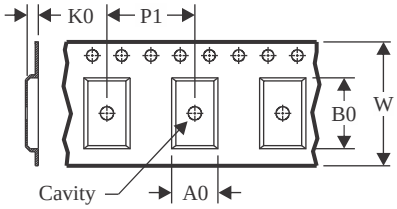
TAPE AND REEL INFORMATION

REEL DIMENSIONS

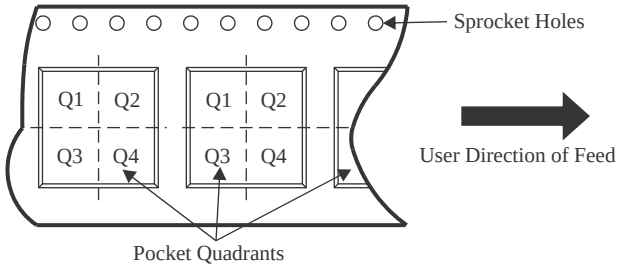


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

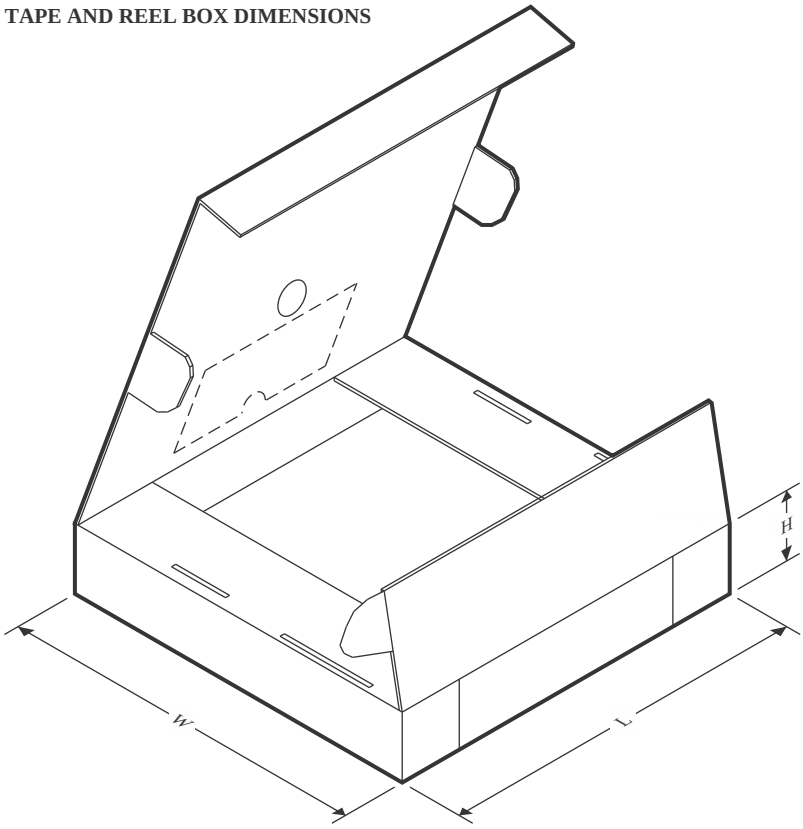
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

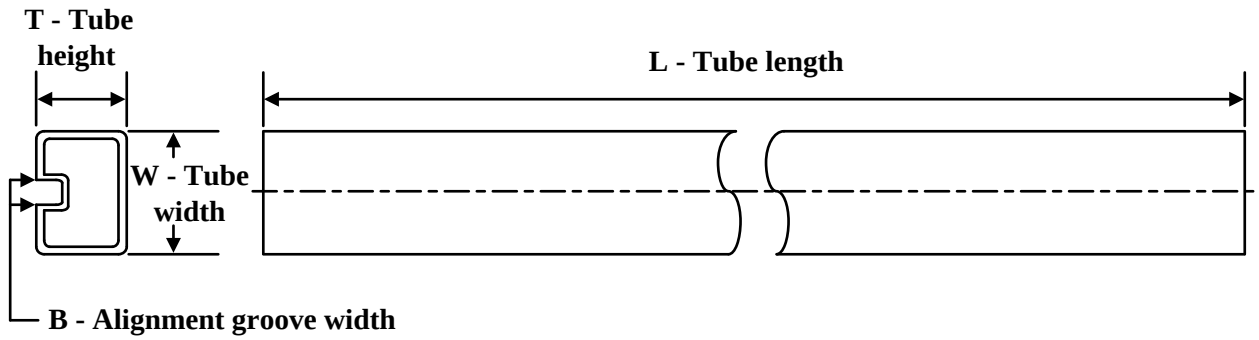
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

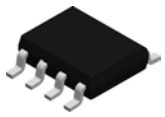
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1176DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75HVD1176DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD1176D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD1176DG4	D	SOIC	8	75	507	8	3940	4.32
SN75HVD1176D	D	SOIC	8	75	507	8	3940	4.32

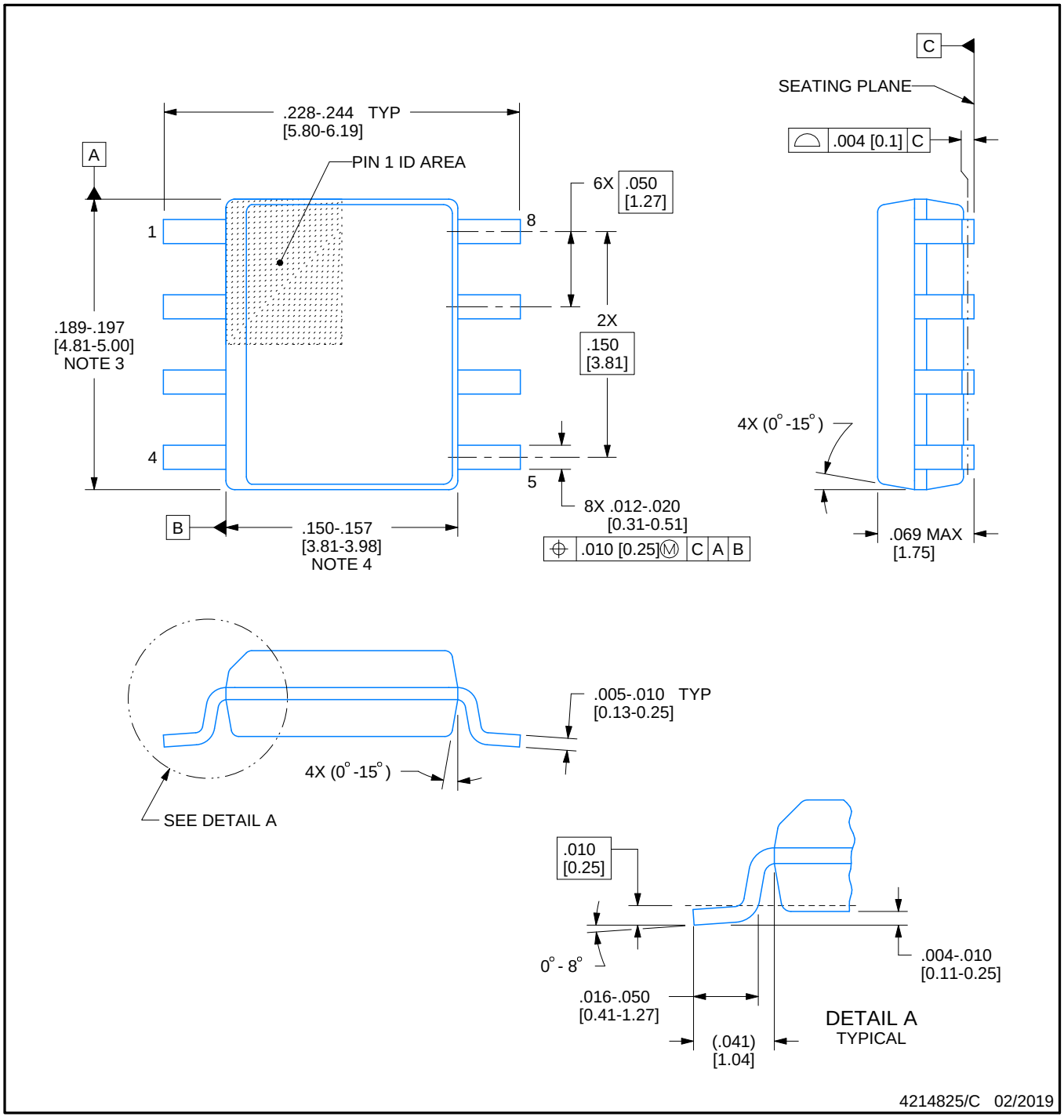


PACKAGE OUTLINE

D0008A

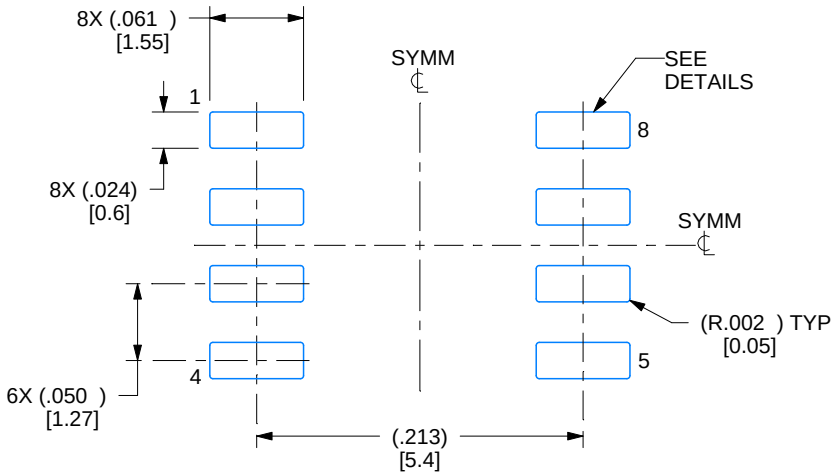
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

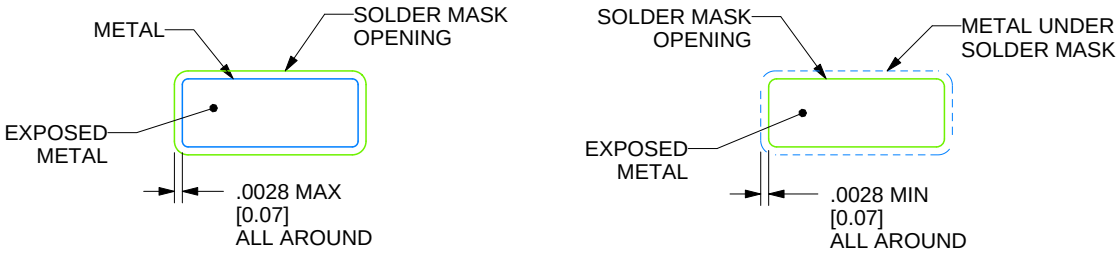


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

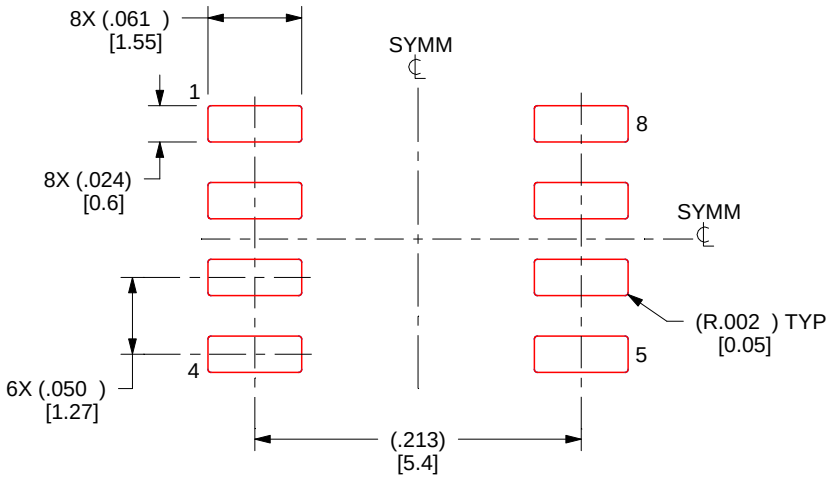
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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